

Model Name : VILE1 & VILE2  
File Name : NM-A043, NM-A044  
BOM P/N:


www.rosefix.com

VILE1:

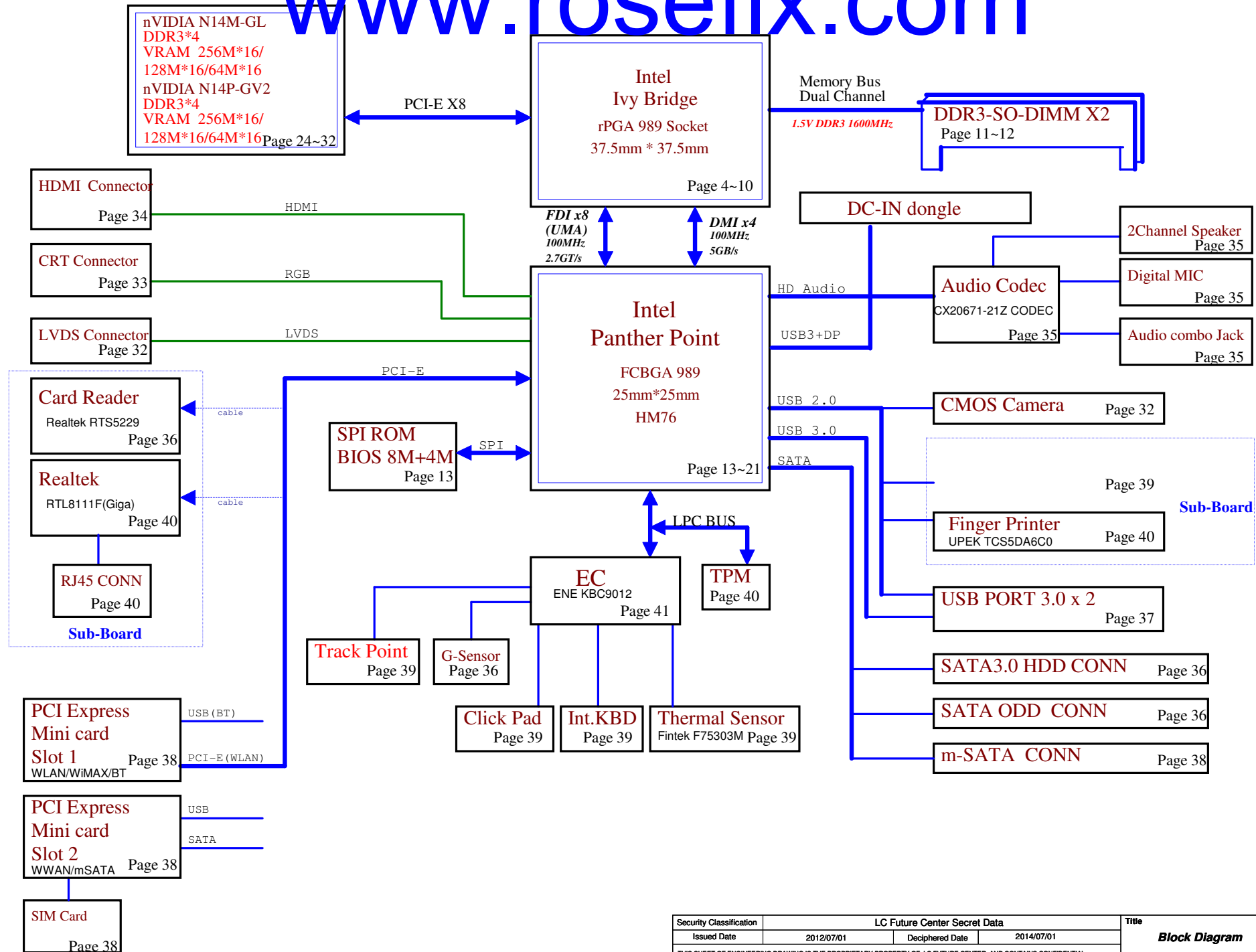
VILE2:

M/B Schematics Document  
Intel Ivy Bridge Processor with DDRIII + Panther Point PCH  
GPU nVIDIA N14M-GL / N14P-GV2

2012-11-07  
REV:0.1

www.vinafix.vn



## Voltage Rails

power plane	State	+B	+5VALW	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS <b>+0.75VS</b> <b>+1.05VS</b>	+3VM +1.05VM
S0		○	○	○	○	○	○ M3 Supported
S3		○	○	○	○	✗	○ M3 Supported
S5 S4/AC		○	○	✗	✗	✗	○ M3 Supported
S5 S4/ Battery only		✗	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist		✗	✗	✗	✗	✗	

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

## EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M1001_101xb	

## PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

## SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	✓ +3VALW	X	X	X	X	X
SMB_EC_DA1	+3VALW							
SMB_EC_CK2	KB9012	X	X	X	X	X	X	✓ +3VS
SMB_EC_DA2	+3VALW							
SMBCLK	PCH	X	X	X	✓ +3VS	✓ +3VS	X	X
SMBDATA	+3VALW							
SMLOCLK	PCH	X	X	X	X	X	X	X
SMLODATA	+3VALW							
SML1CLK	PCH	✓ +3VS	X	✓ +3VS	X	X	✓ +3VS	X
SML1DATA	+3VALW							

STATE	SIGNAL	S1#	S2#	S3#	S4#	LP_S	+VALW	+V	+VS	CLK
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

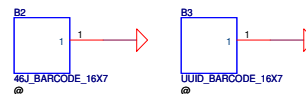
## USB Port Table

	USB 2.0 Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0 1 2 3 4 5 6 7
	UHCI1	2 3 4 5 6 7
	UHCI2	4 5 6 7
	UHCI3	5 6 7
	UHCI4	8 9 10 11 12 13
	UHCI5	9 10 11 12 13
EHCI2	UHCI6	10 11 12 13
	UHCI7	11 12 13
	UHCI8	12 13
	UHCI9	13

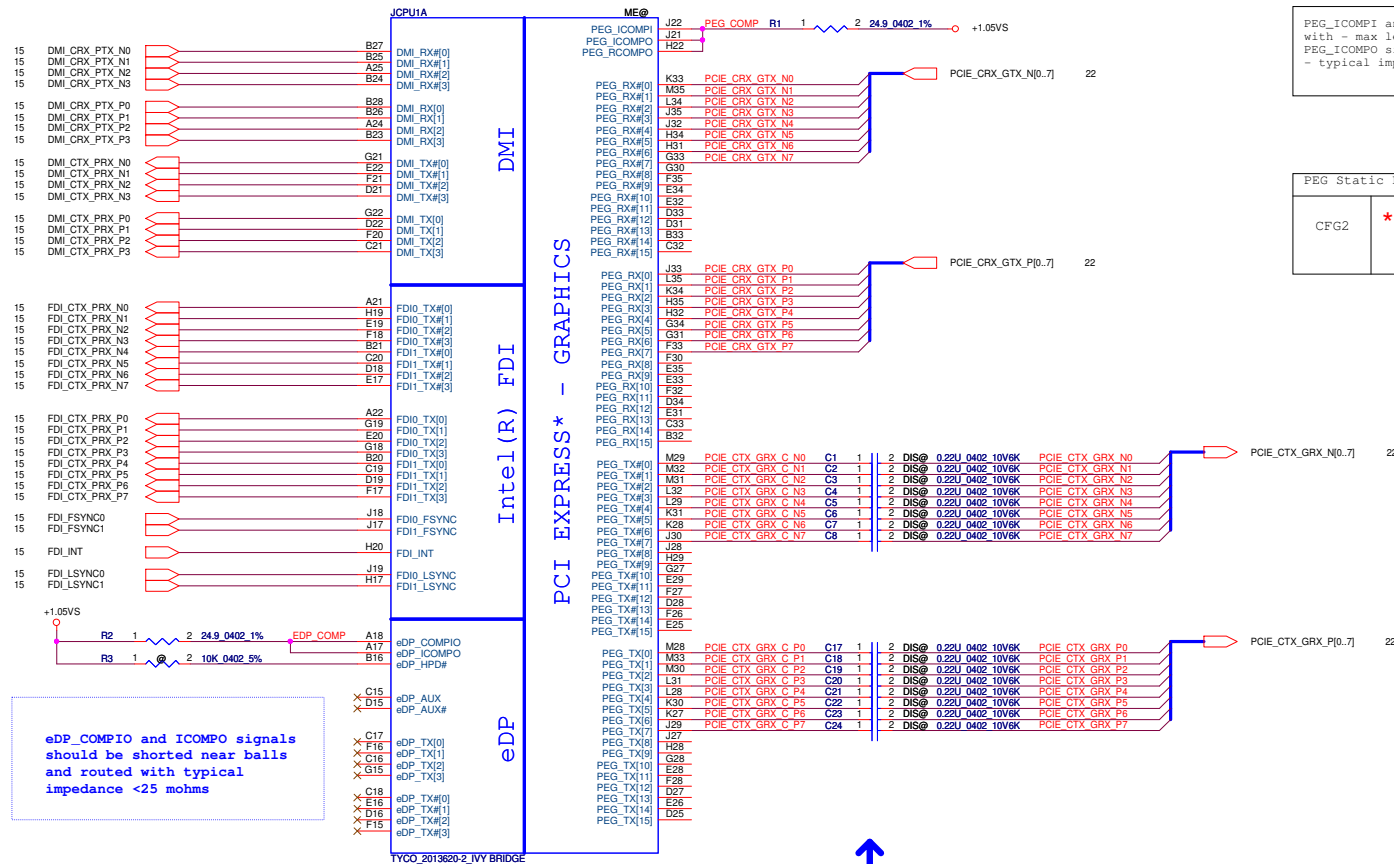
## BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
Nvidia	DIS@
PCH AUX Power	+3V_PCH@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N14M-GL	N14MGL@
GPU N14P-GV2	N14PGV2@
SIM Card Slot	3G@
Touch Panel	Touch@
Finger Print Board	FP@
SSD	SSD@

ZZZ5  
DA PCB  
DA8000TG00  
NM-A043



Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Notes List
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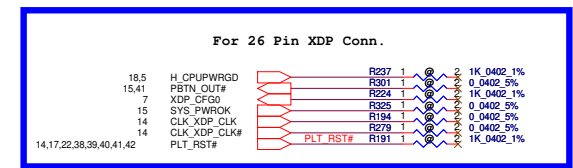
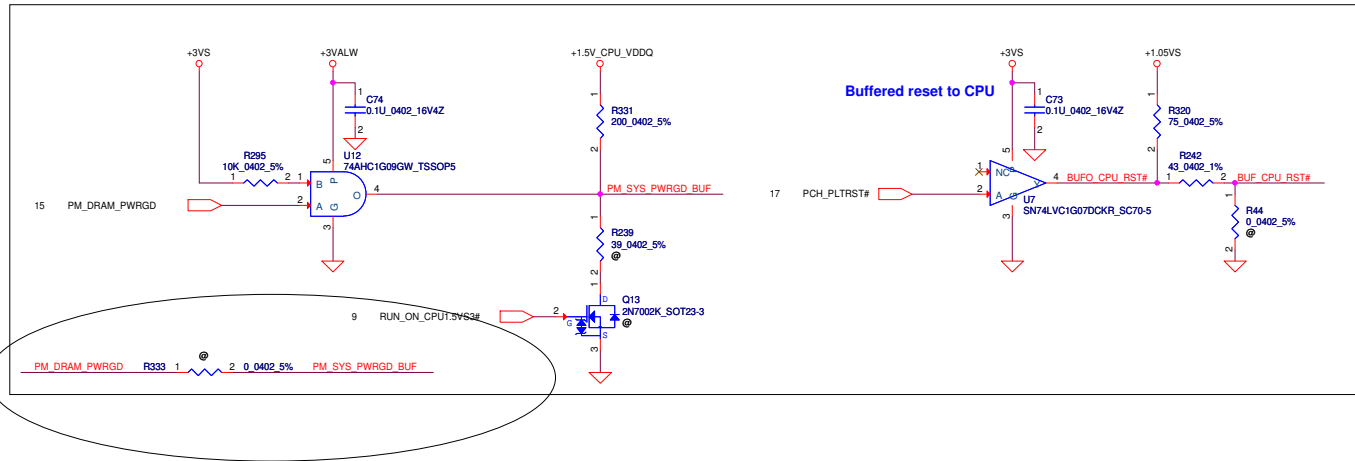
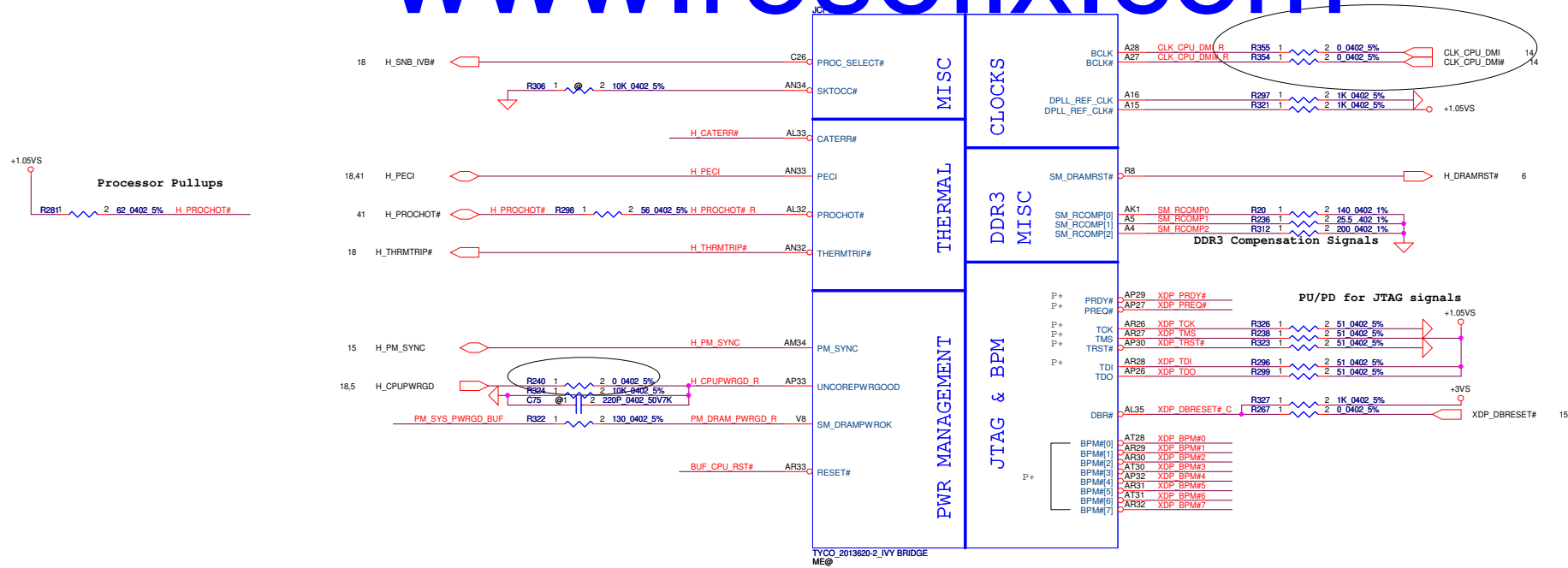
PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

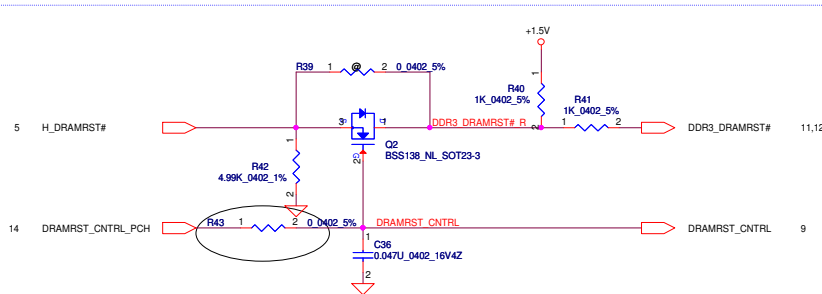
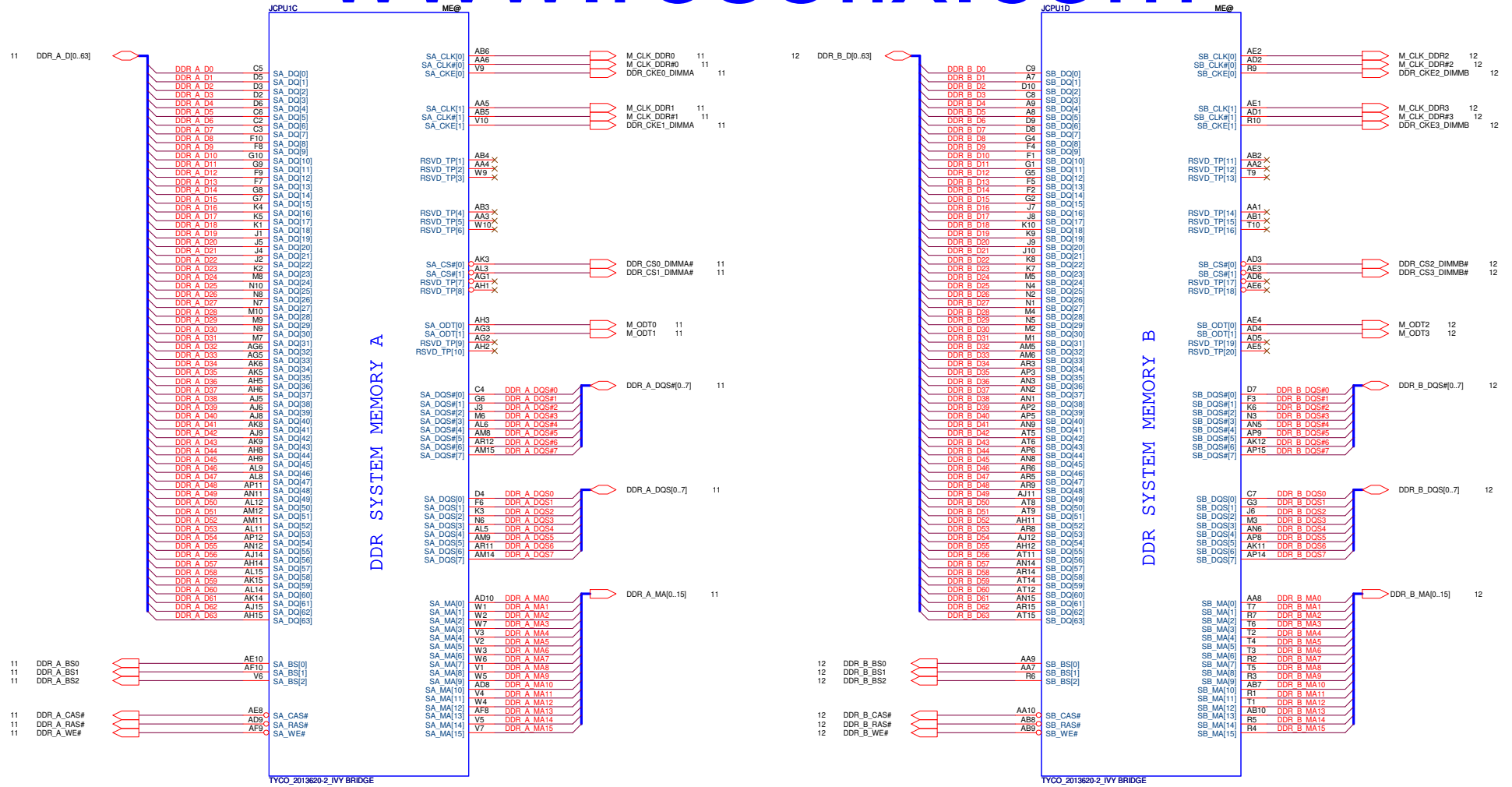
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
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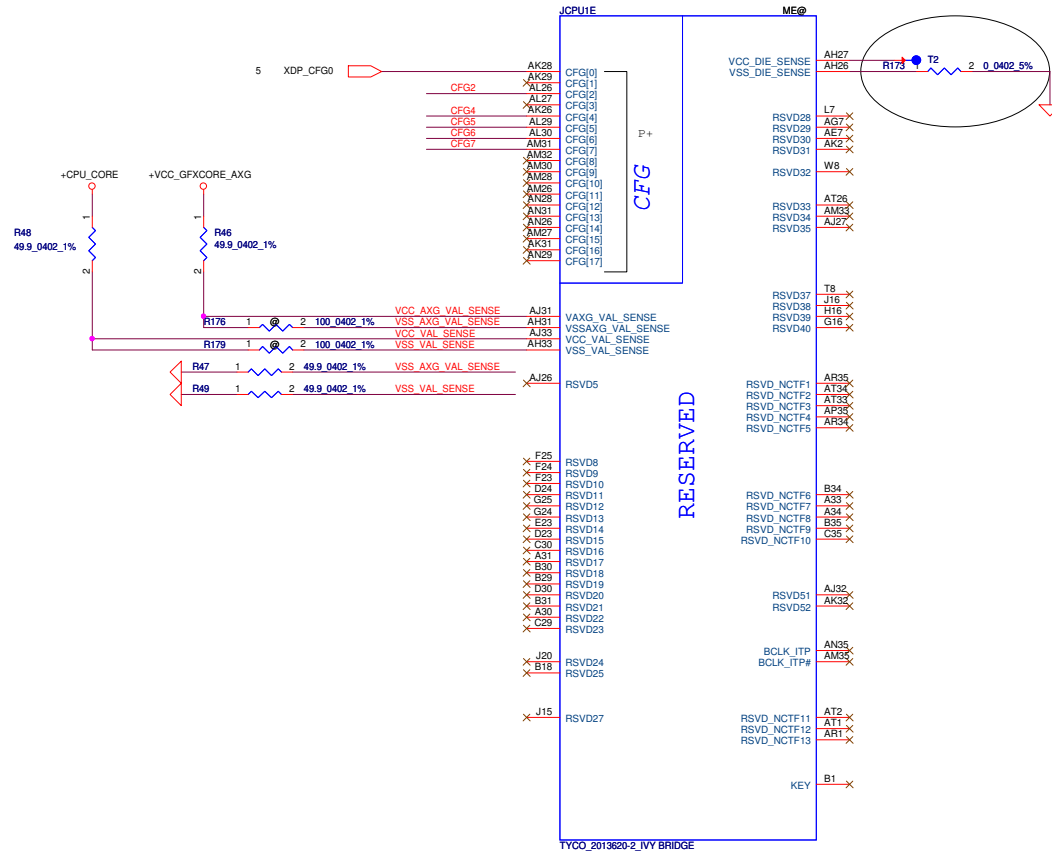
eDP\_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Nvidia support PCIe Gen2

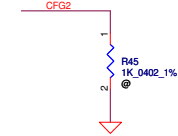




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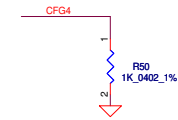


## CFG Straps for Processor



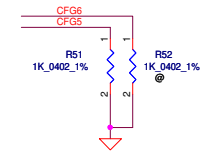
### PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>
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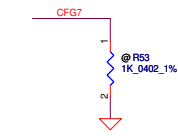
### Display Port Presence Strap

CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
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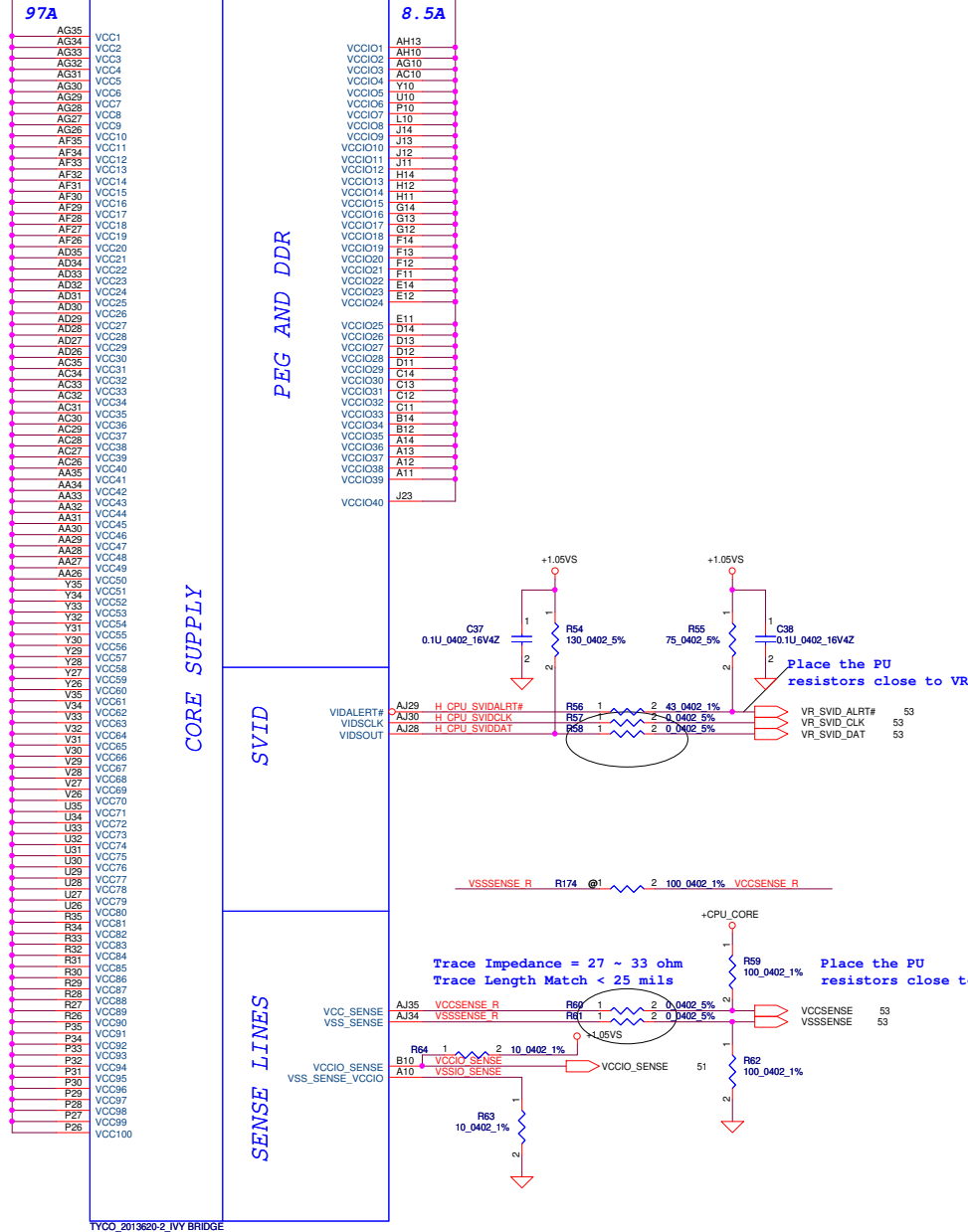
### PCIe Port Bifurcation Straps

CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>★ 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled; function 2 enabled)</p> <p>00: x8, x4, x4 - Device 1 functions 1 and 2 enabled</p>
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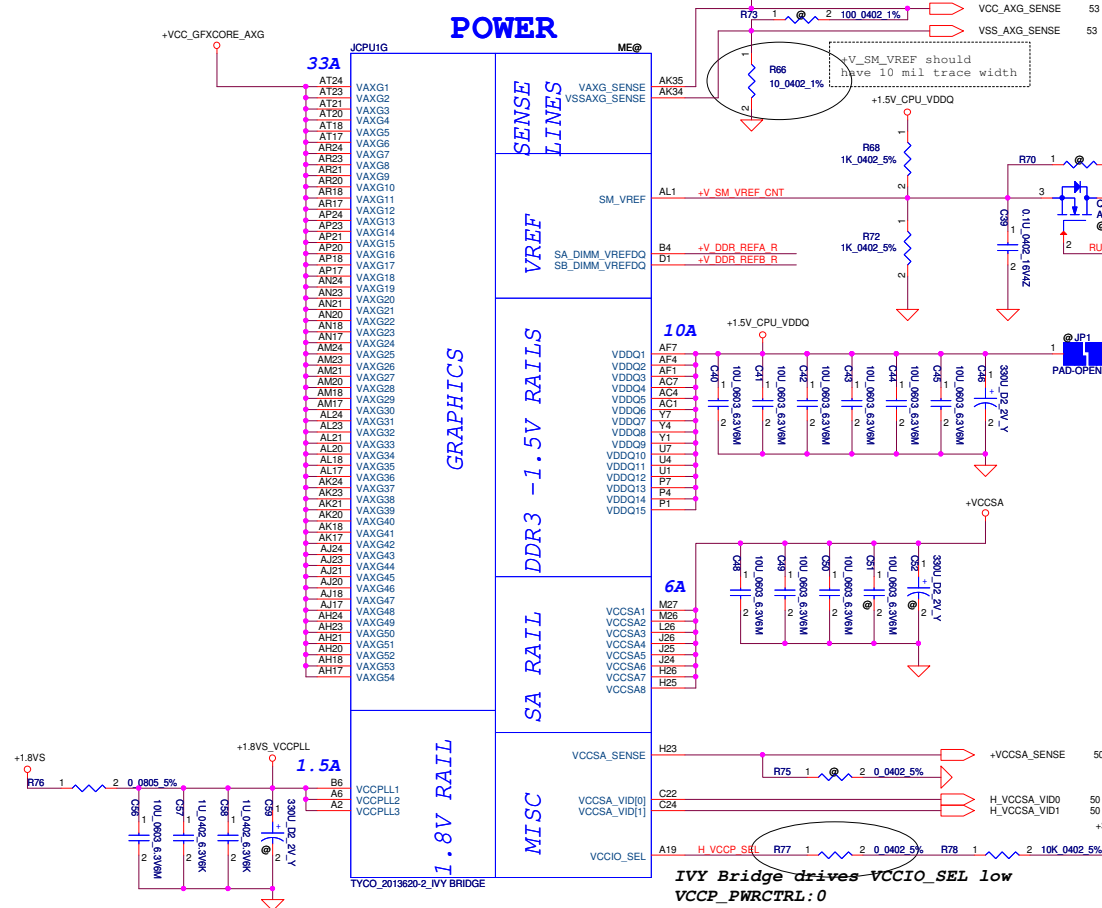


### PEG DEFER TRAINING

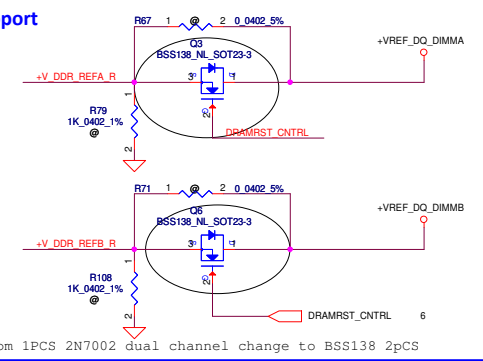
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
------	--







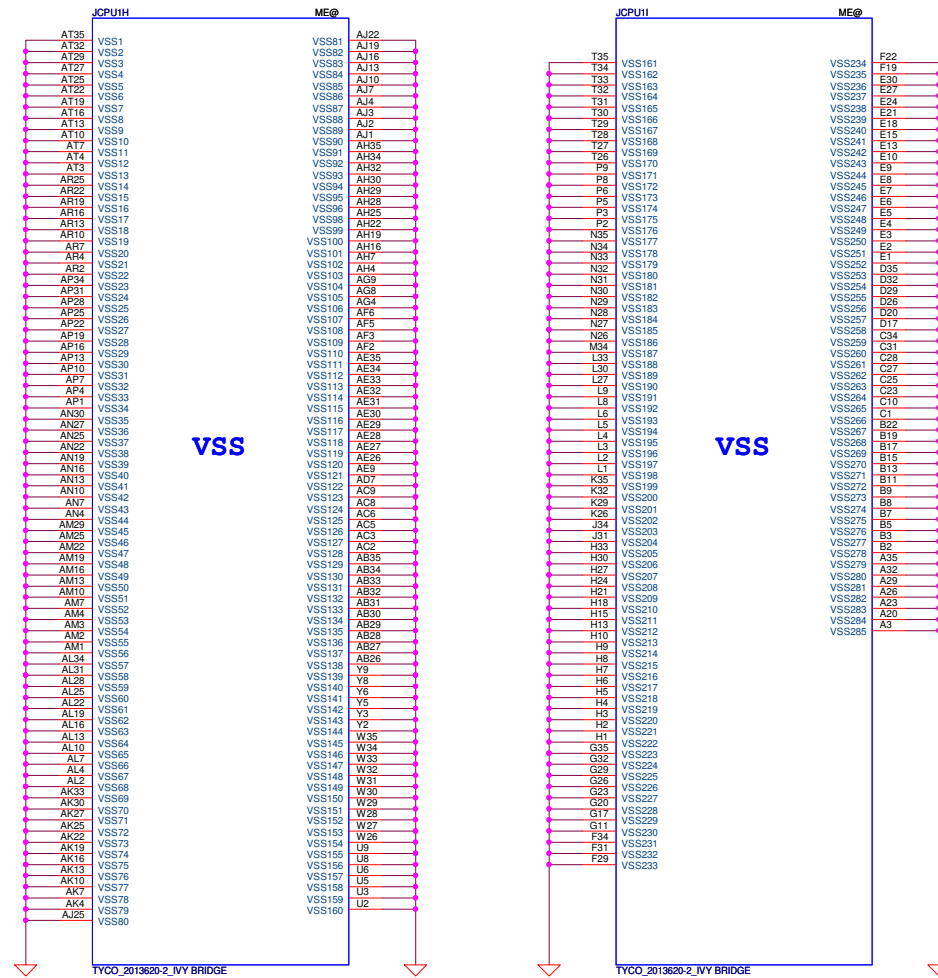
## M3 Support

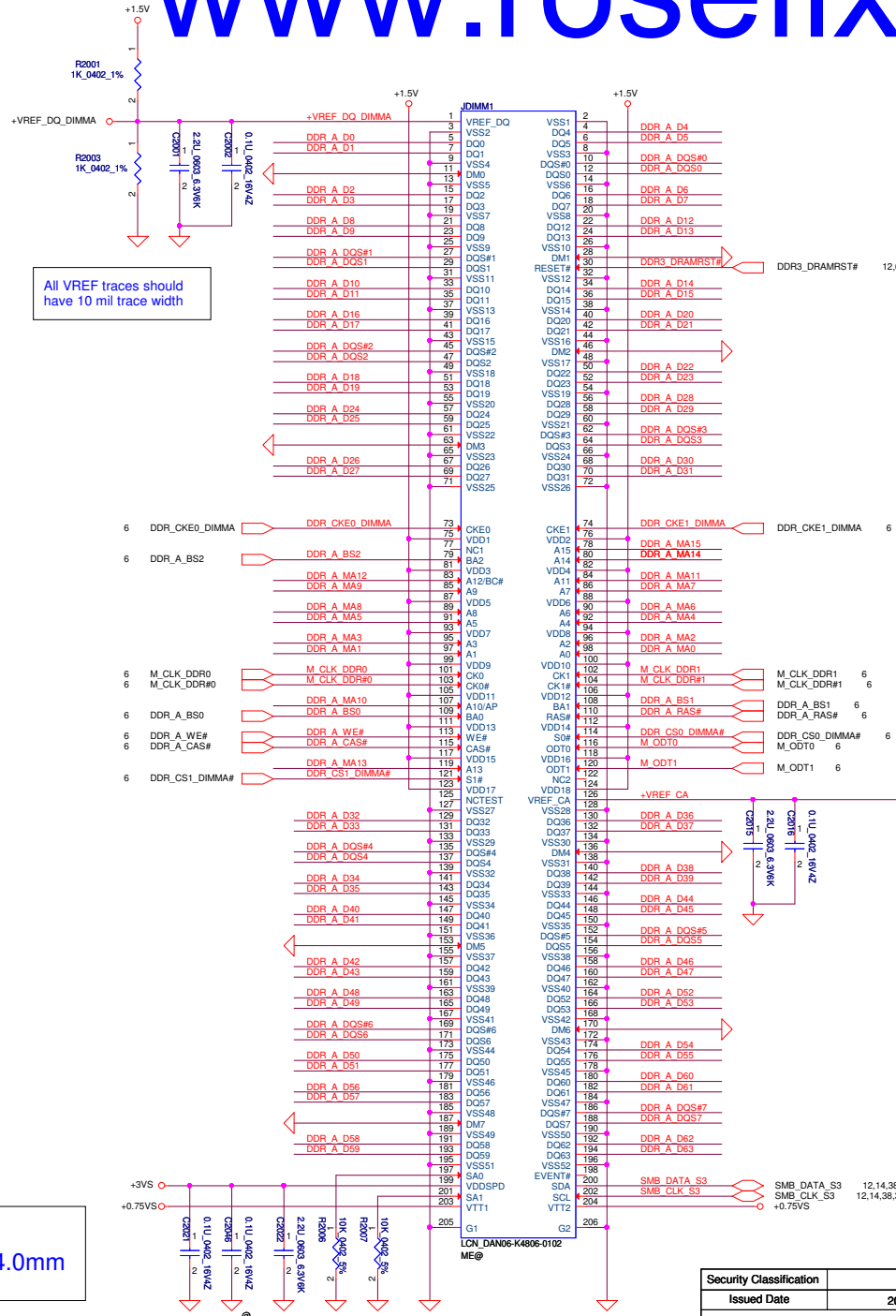


**Vaxg**

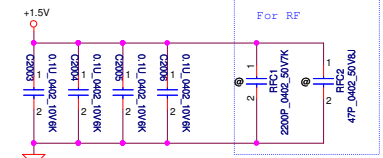
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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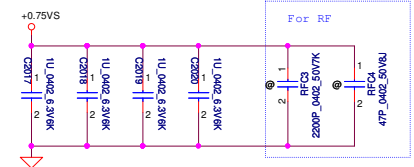




Layout Note:  
Place near  
JDIMM1



Layout Note:  
Place near  
JDIMM1.203,204



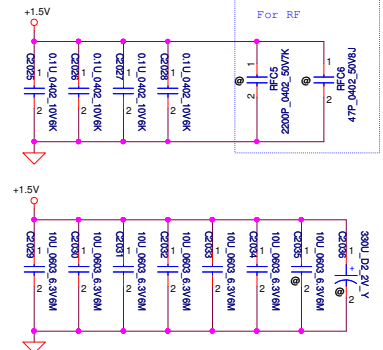
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For RF

2200P\_0402\_50V7K

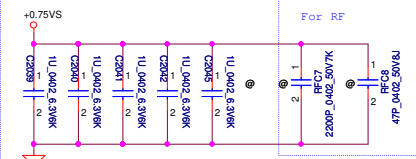
47P\_0402\_50V8J




For RF

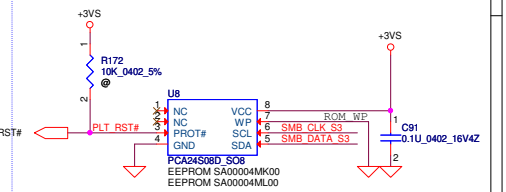
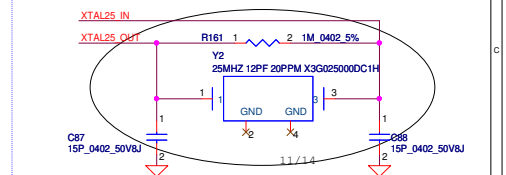
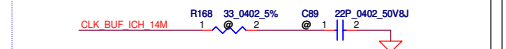
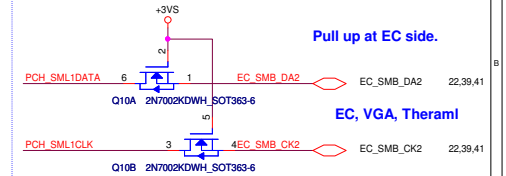
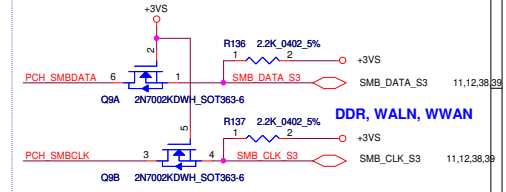
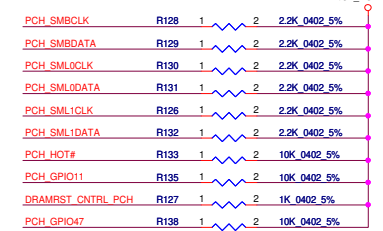
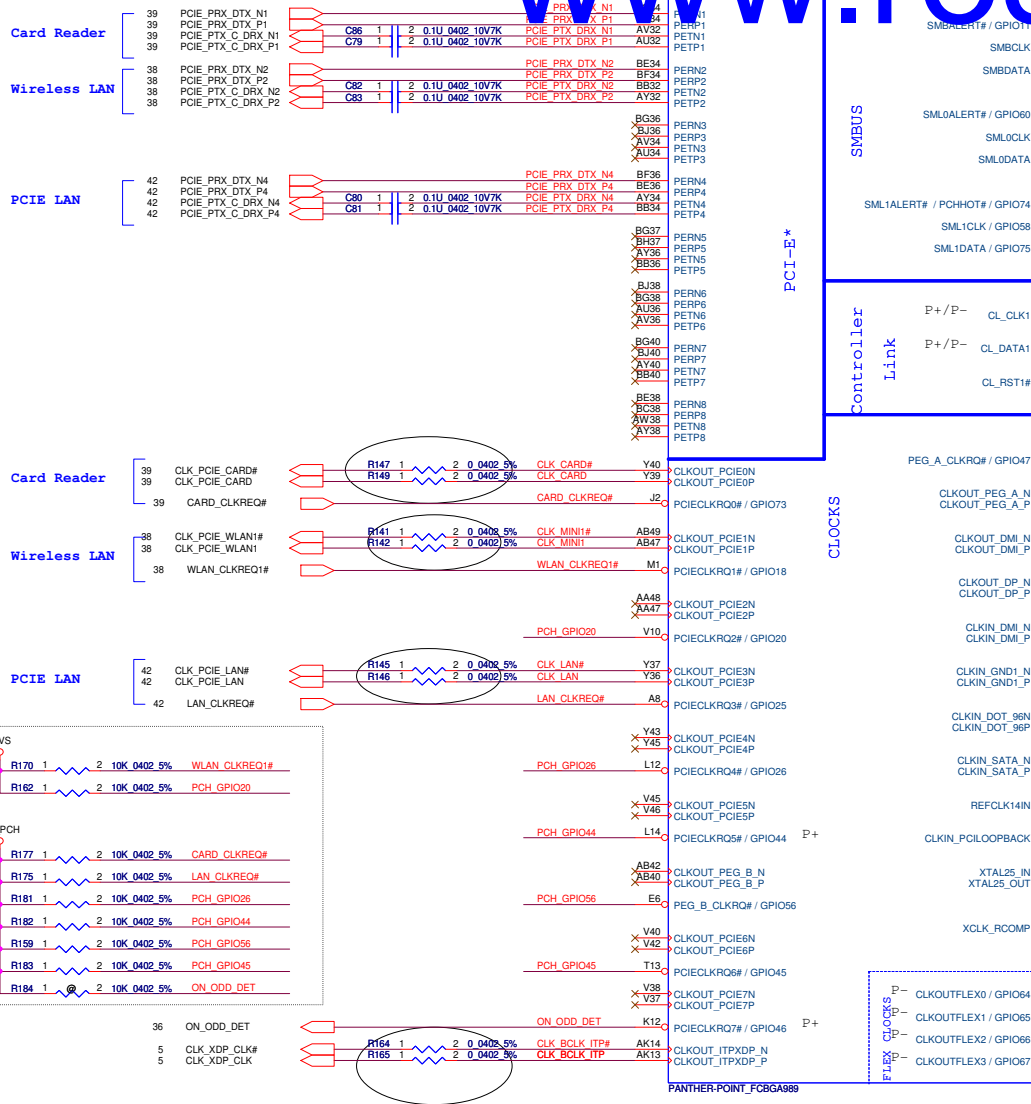
220P\_0402\_50V7K  
RFC7


47P\_0402\_50V8J  
RFC8



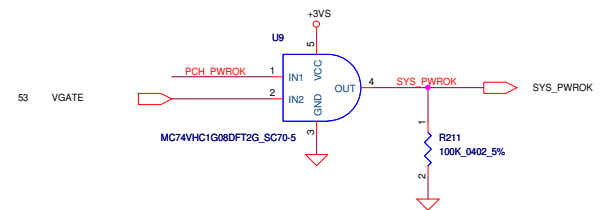
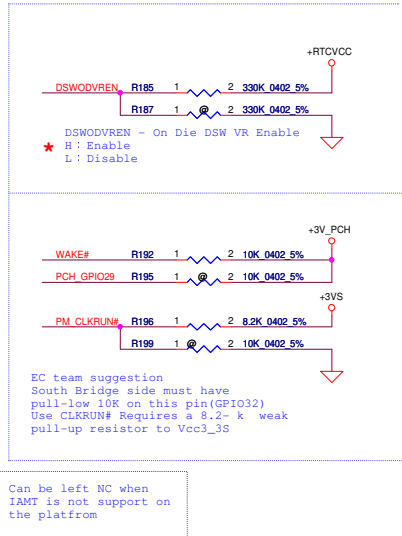
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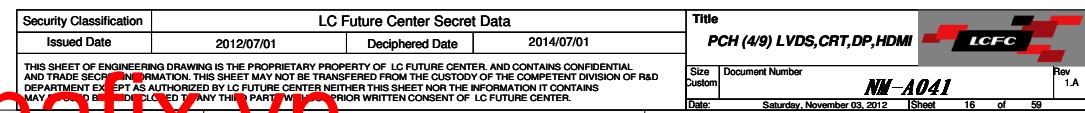


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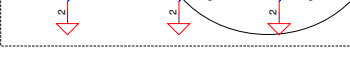
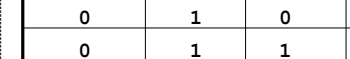
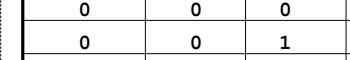
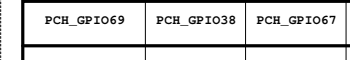
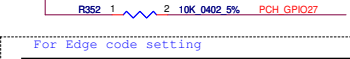
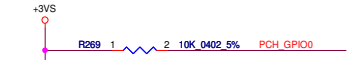
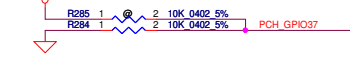
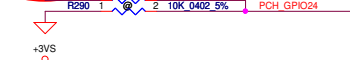
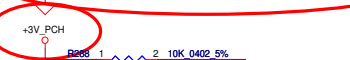
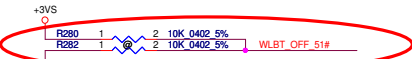
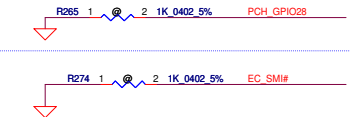
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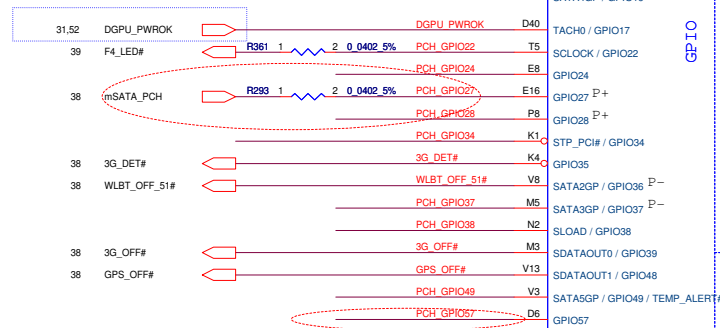




**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
★ H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable



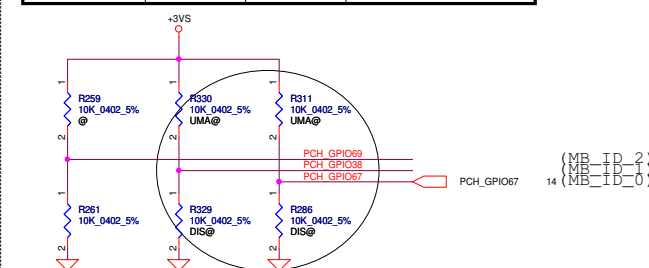
For GC6



GPIO34

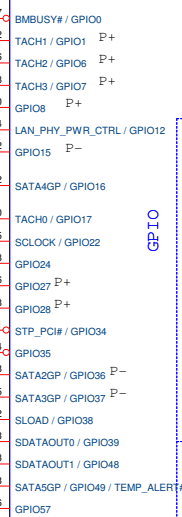
For Edge code setting

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA



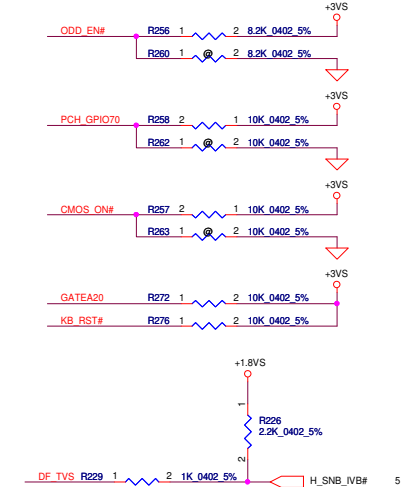
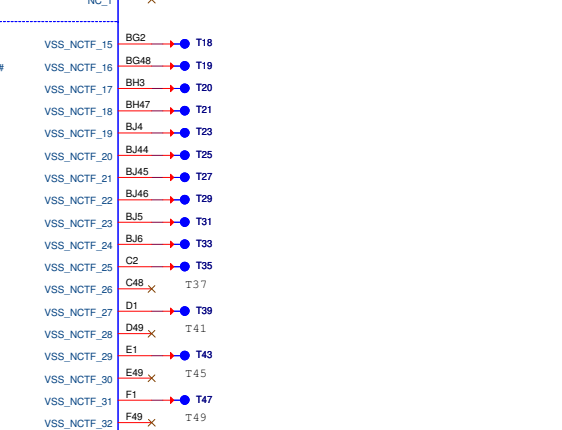
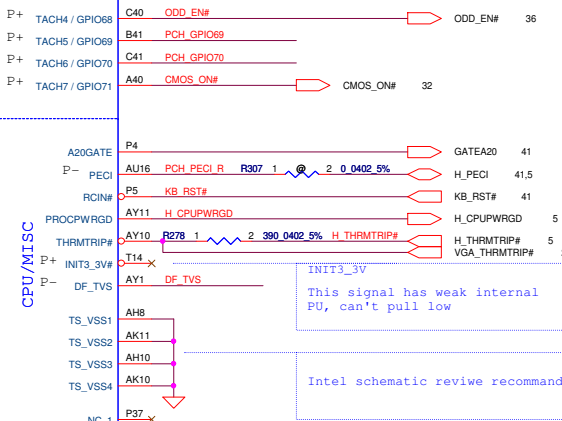
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USF



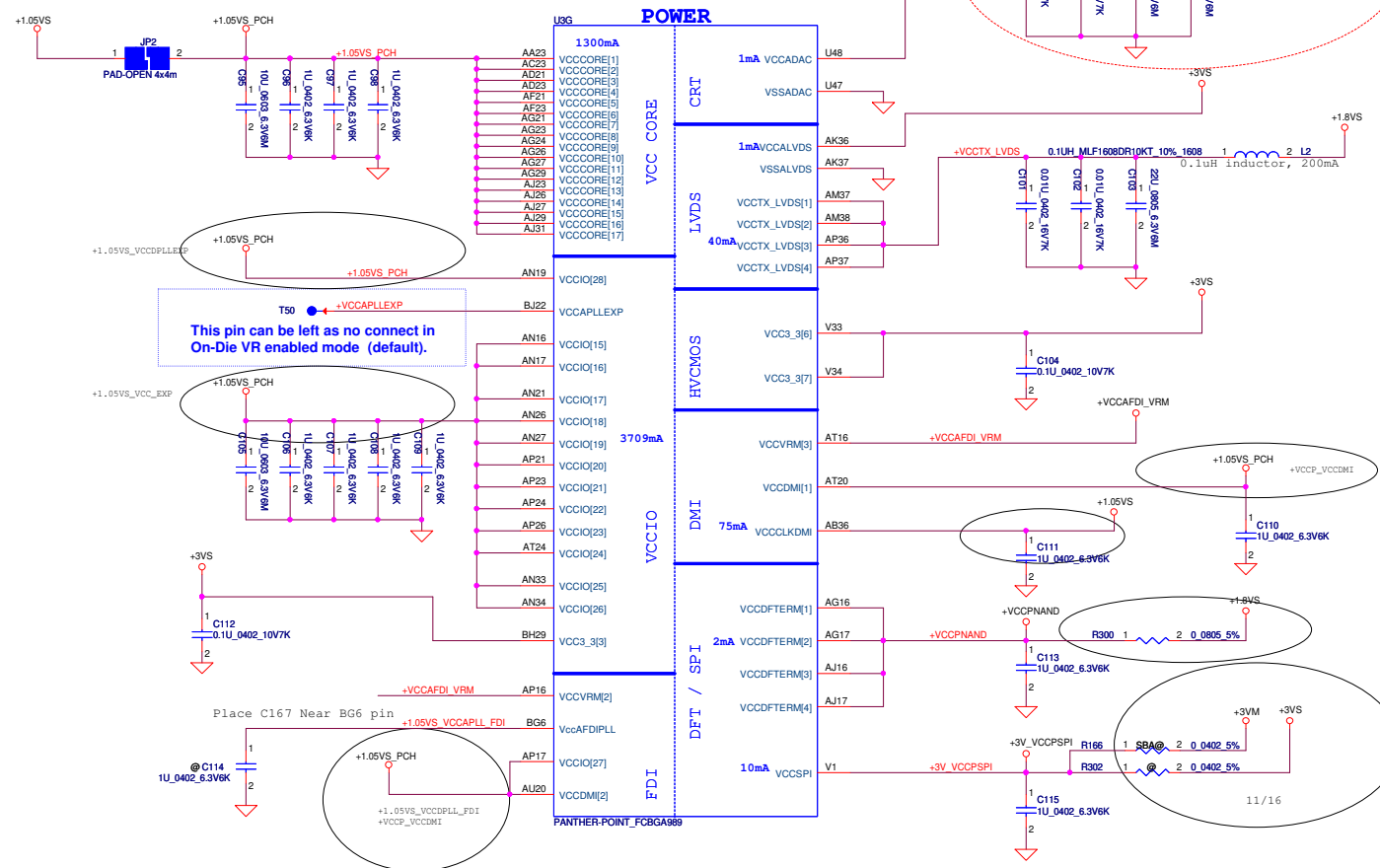
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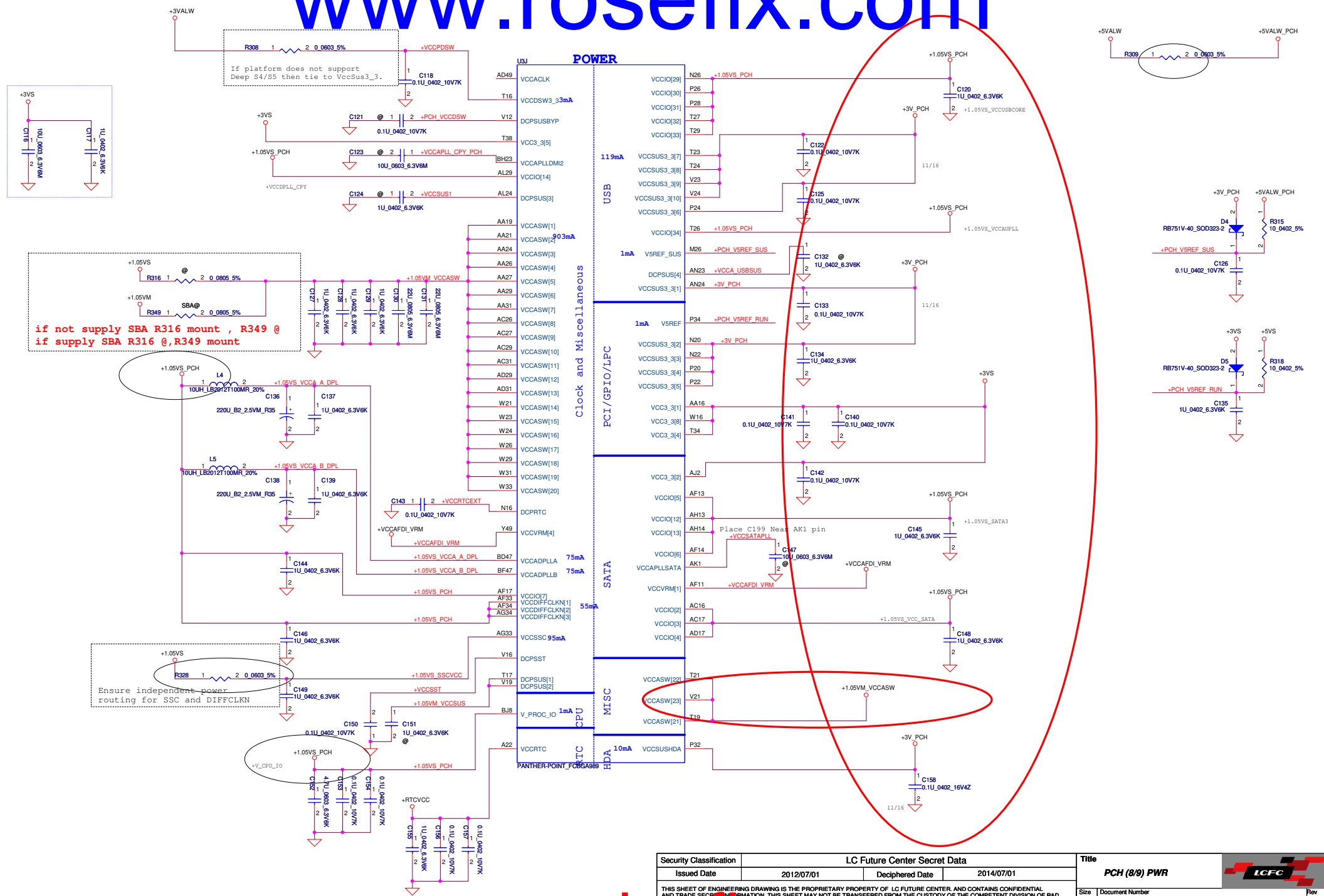
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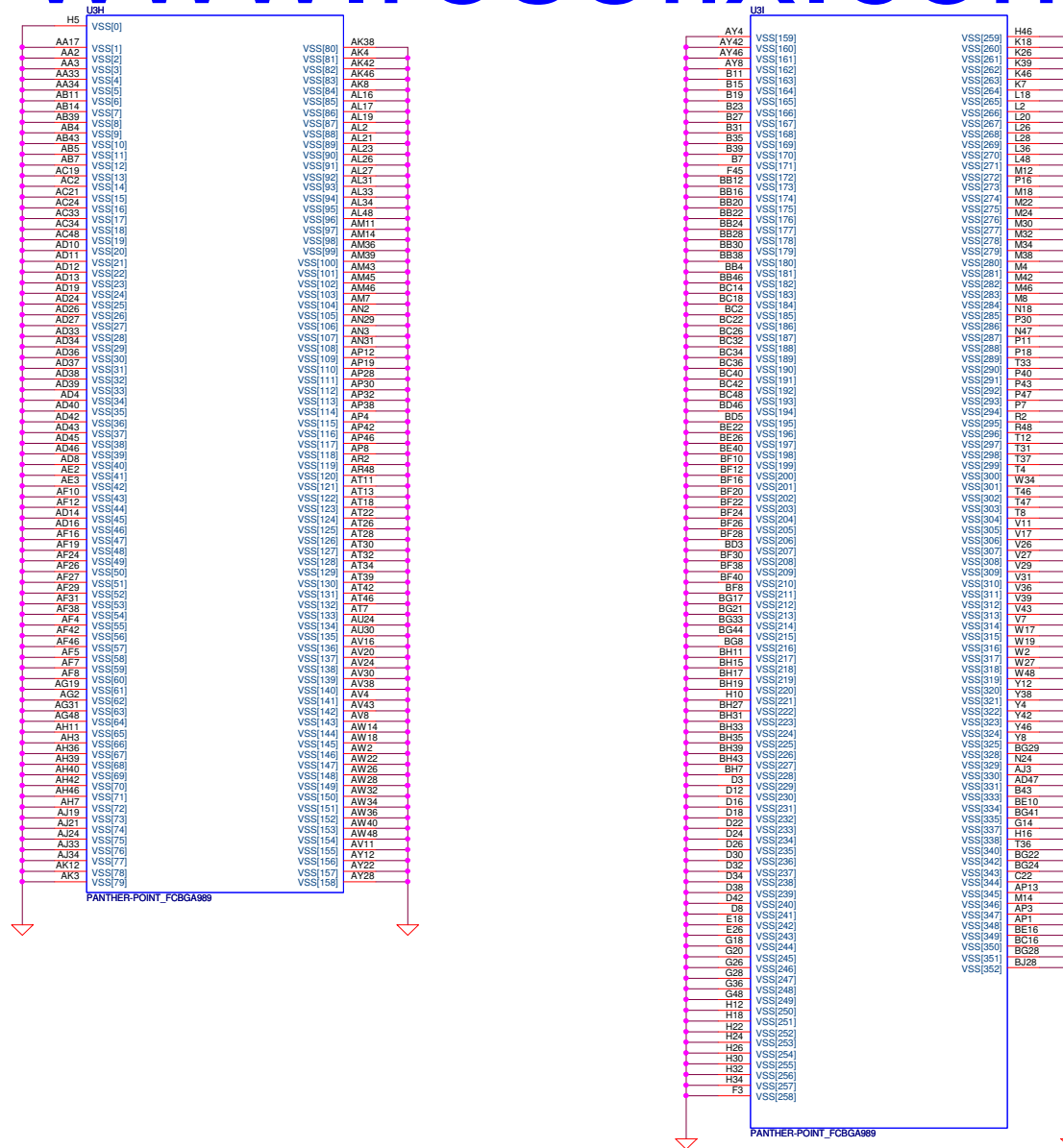


DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH Set to Vss when LOW

CLOSE TO THE BRANCHING POINT










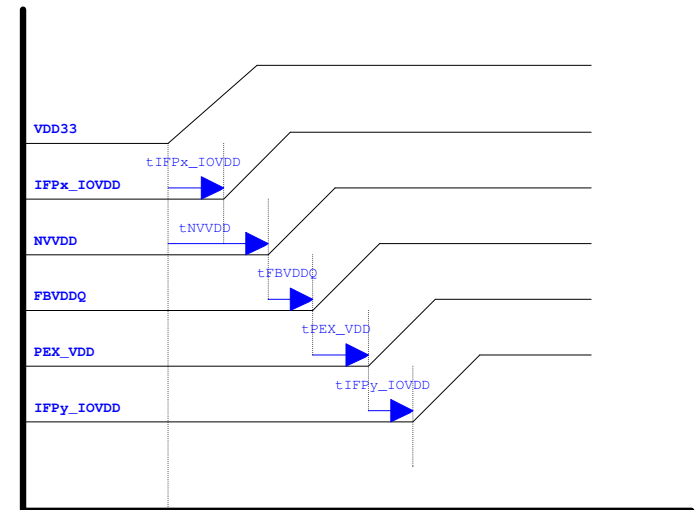
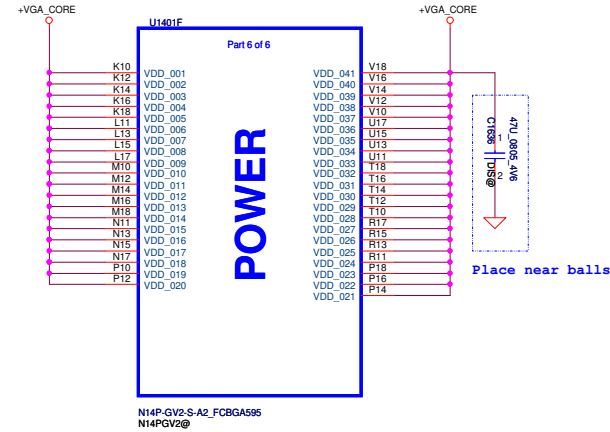
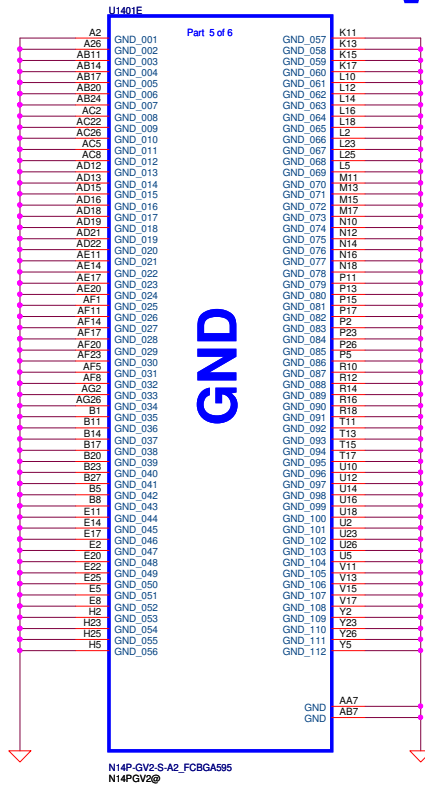


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Issued Date	2012/07/01	Deciphered Date	2014/07/01	N14P_LVDS/HDM/THERM	
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Size	Custom	Document Number	NW-A041		Rev 1.A
Date:	Thursday, November 01, 2012		Sheet	23	of 59








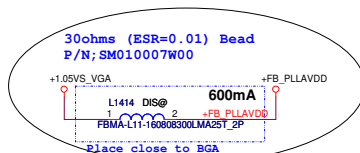
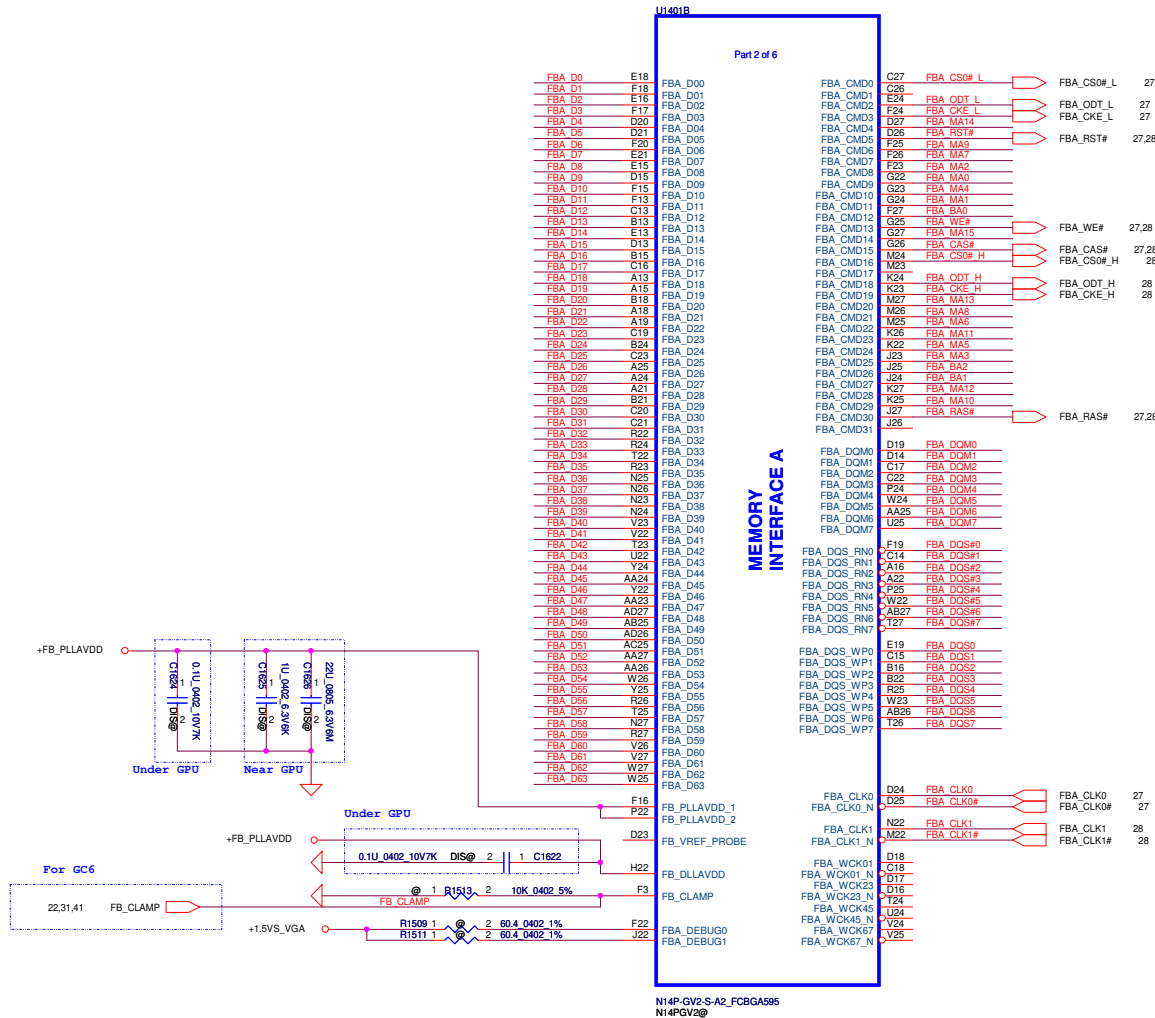



NV Recommended Power On Sequencing Order

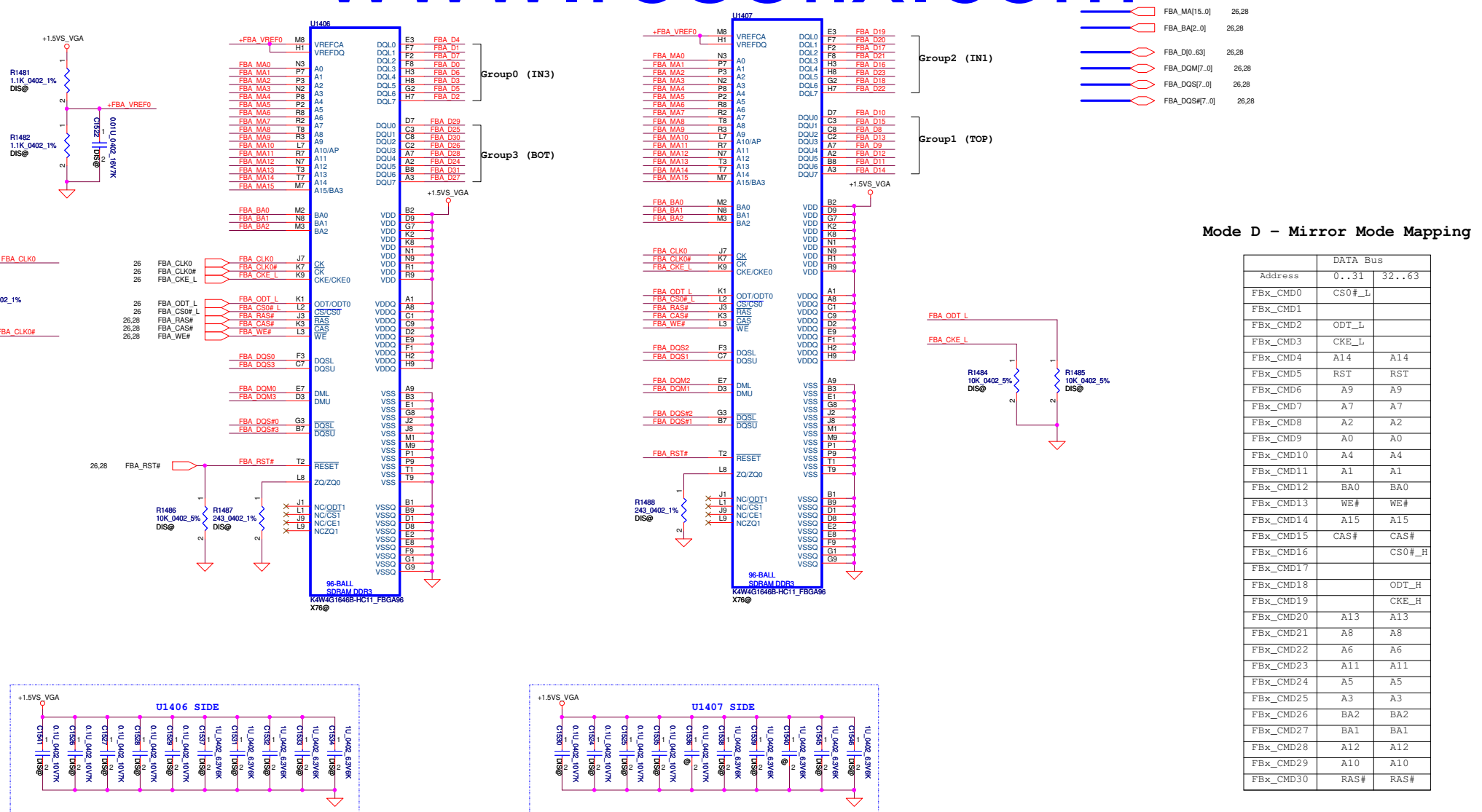
X=A and B  
Y=C, D, E and F

Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	N14P_VGA CORE, GND		
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				Custom	NW-A041	
				Date:	Thursday, November 01, 2012	Sheet 25 of 59

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

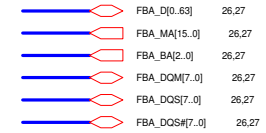
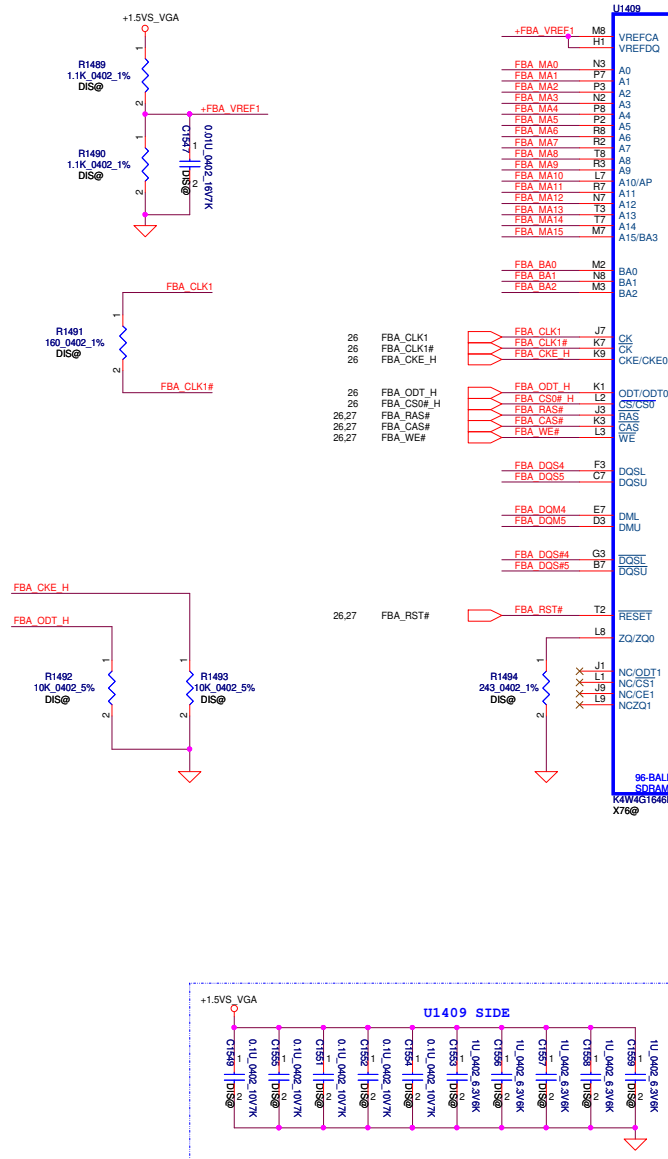


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Issued Date		2012/07/01		Deciphered Date		2014/07/01		N14P_MEM Interface			
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Date: Thursday, November 01, 2012										Sheet 26 of 59	



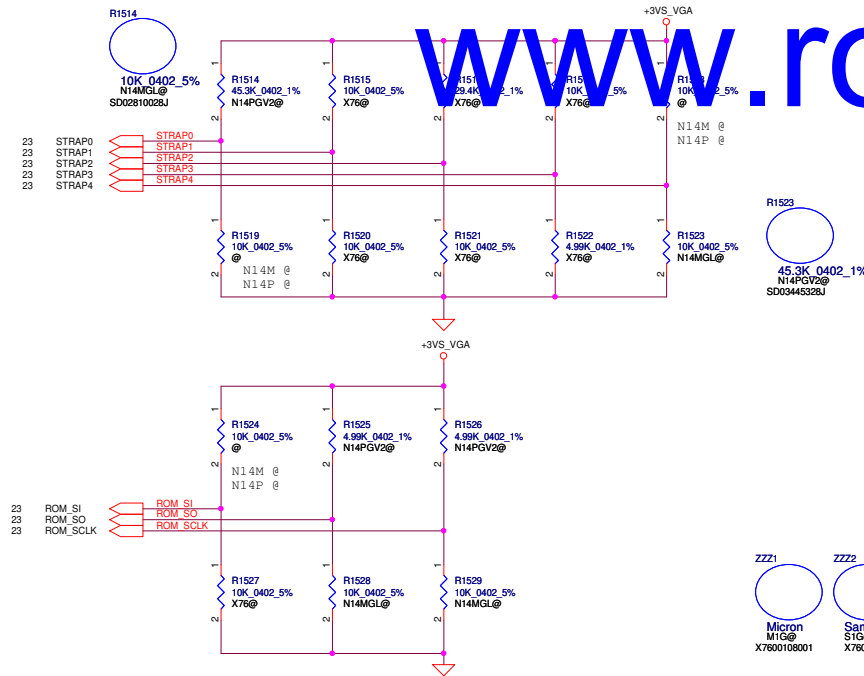
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

## Memory Partition A - Upper 32 Bits



### Mode D - Mirror Mode Mapping

Address	DATA Bus
FBx_CMD0	CS0#_L
FBx_CMD1	ODT_L
FBx_CMD2	CKE_L
FBx_CMD3	A14
FBx_CMD4	A14
FBx_CMD5	RST
FBx_CMD6	A9
FBx_CMD7	A7
FBx_CMD8	A2
FBx_CMD9	A0
FBx_CMD10	A4
FBx_CMD11	A1
FBx_CMD12	BA0
FBx_CMD13	WE#
FBx_CMD14	A15
FBx_CMD15	CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	ODT_H
FBx_CMD18	CKE_H
FBx_CMD19	A13
FBx_CMD20	A8
FBx_CMD21	A6
FBx_CMD22	A11
FBx_CMD23	A5
FBx_CMD24	A3
FBx_CMD25	BA2
FBx_CMD26	BA1
FBx_CMD27	A12
FBx_CMD28	A10
FBx_CMD29	RAS#
FBx_CMD30	RAS#



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SI	+3VS_VGA	PCI_DEV[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SO	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP0	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP1	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP2	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP3	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP4	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
		PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User [3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation

DP_PLL_VDD33V	
0	Reserved
1	Default


GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A	PU 5K	PU 5K	PD 45K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		128Mx16								
	Micron 1000MHz	MT41J128M16JT-093G	PU 5K	PU 5K	PD 30K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		128Mx16								
	Samsung 900MHz	K4W4G1646B-HC11	PU 5K	PU 5K	PD 20K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		256Mx16								
	Micron 900MHz	MT41K256M16HA-107G	PU 5K	PU 5K	PD 10K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		256Mx16								

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14M-GL	Samsung 1000MHz	K4W2G1646E-BC1A	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K
		128Mx16								
	Hynix 1000MHz	H5TQ2G63DFR-N0C	PD 10K	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K
		128Mx16								
	Micron 1000MHz	MT41J128M16JT-093G	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K
		128Mx16								
	Samsung 900MHz	K4W4G1646B-HC11	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PU 10K	PD 10K
		256Mx16								
	Hynix 900MHz	H5TQ4G63MFR-11C	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K
		256Mx16								
	Micron 900MHz	MT41K256M16HA-107G	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PU 10K	PD 10K
		256Mx16								

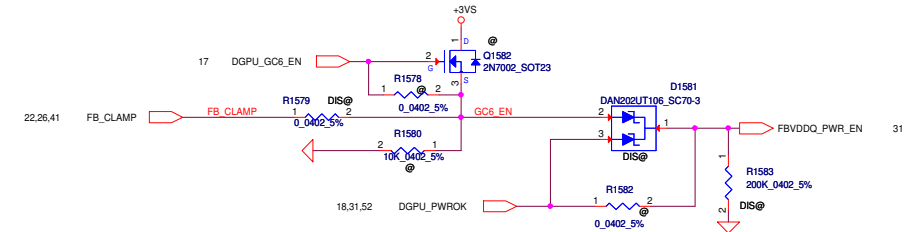
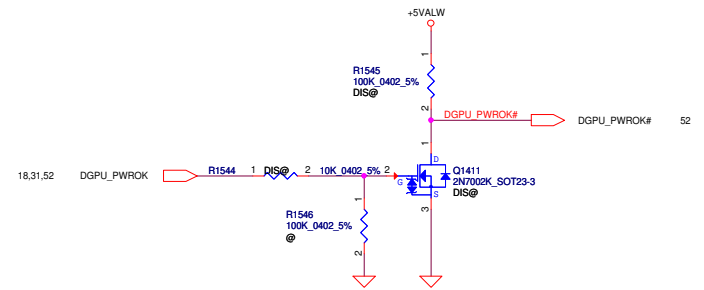
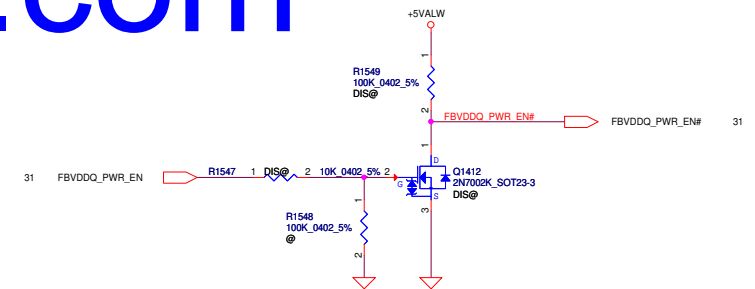


For N14P-GV2 QS Sample  
ROM\_SO change from PU 10K to PU 5K  
ROM\_SCLK change from PD 15K to PU 5K  
STRAP1 change from PD 5K to PD 45K  
STRAP2 change from PU 30K to PD 15K  
STRAP4 change from PD 5K to PD 45K

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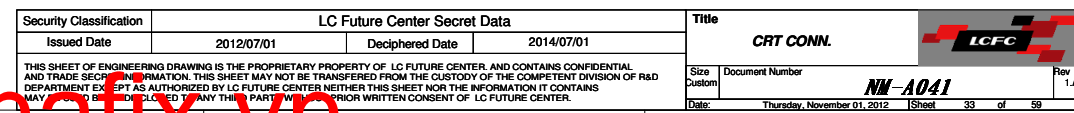
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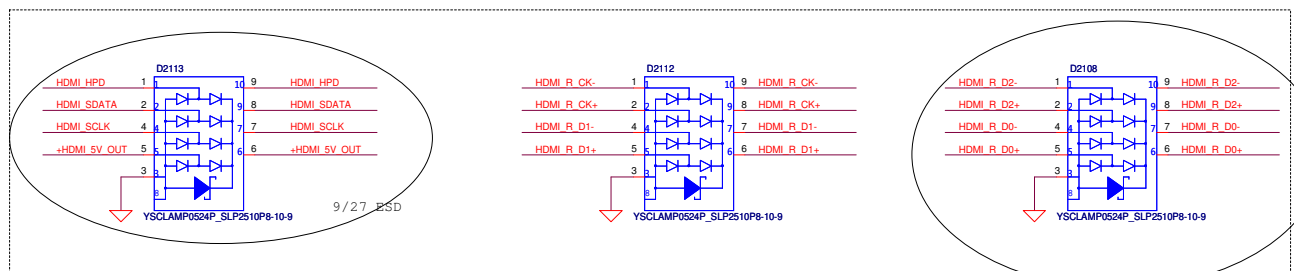
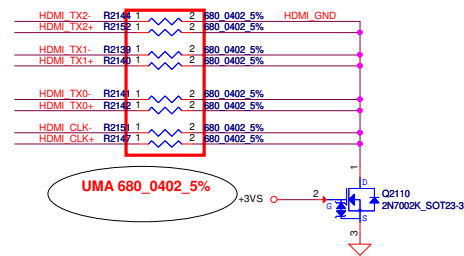
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Issued Date		2012/07/01		Deciphered Date		2014/07/01		LVDS CONN.  Size Custom    Document Number <div style="display: flex; justify-content: space-between; align-items: center;"> <span><b>NW-A041</b></span> <span>Rev 1.1</span> </div>			
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								Sheet		32 of 59	



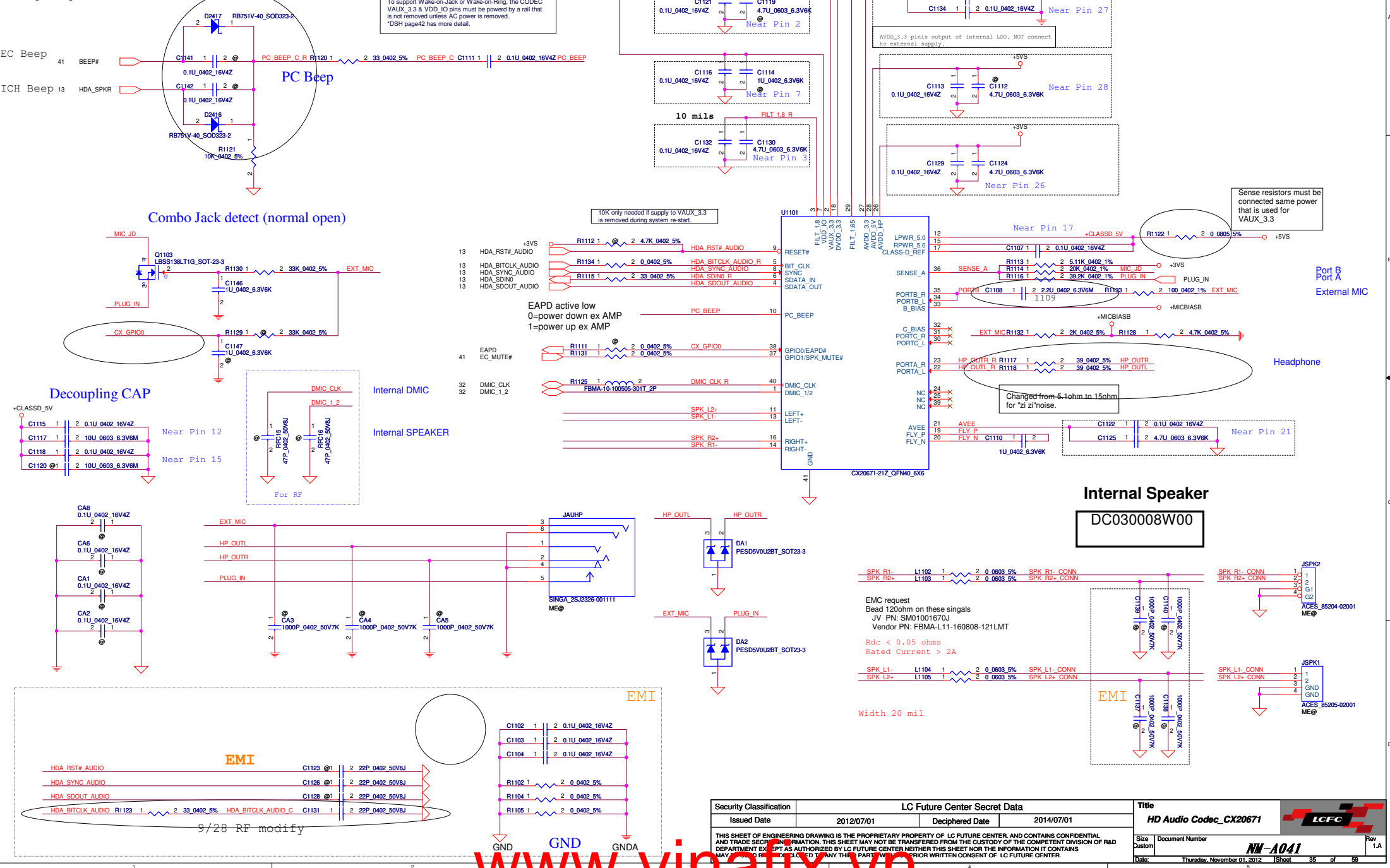





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2012/07/01		2014/07/01		Size Custom		Document Number <b>NW-A041</b>	
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CX20671  
High Definition Audio Codec SoC  
With Integrated Class-D Stereo  
Amplifier.  
An integrated 5 V to 3.3 V Low-dropout  
voltage regulator (LDO).  
An integrated 3.3 V to 1.8V Low-dropout  
voltage regulator (LDO).

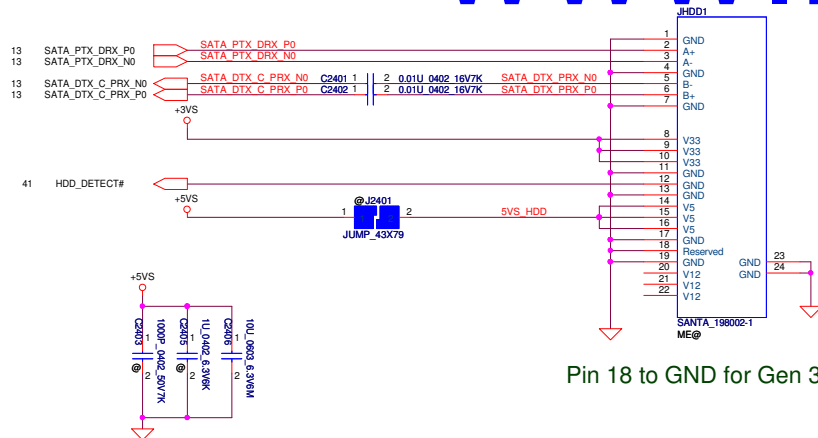
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## SATA HDD CONN.

PN:SP01000HE00

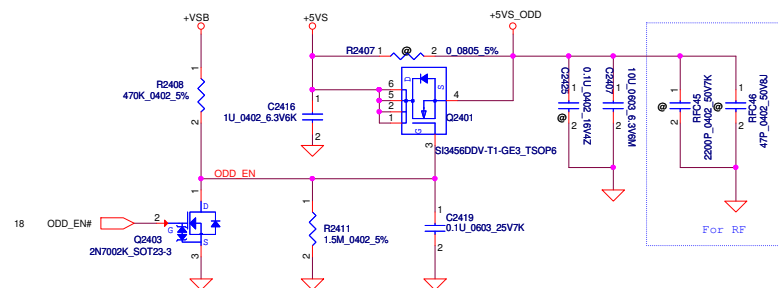
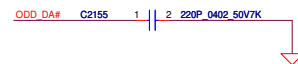
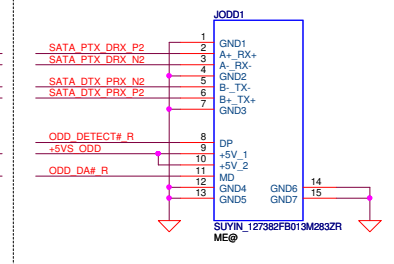
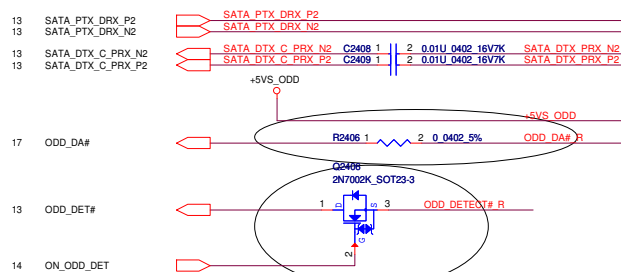


Pin 18 to GND for Gen 3

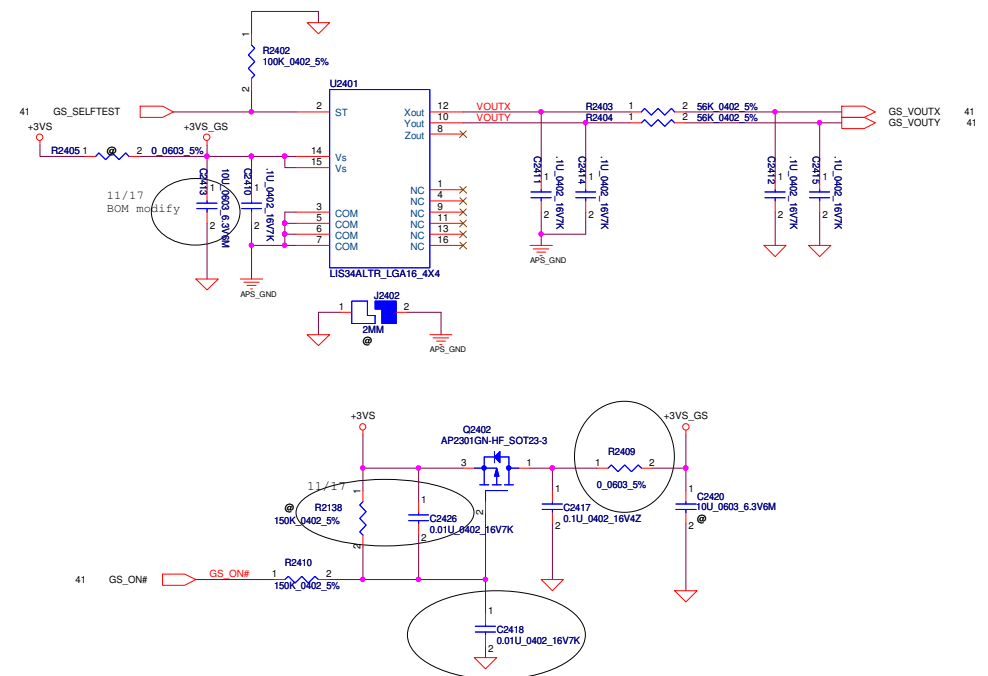
## SATA ODD CONN.


PN:SP01000TU10

for Edge 14''



## APS G-Sensor



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Issued Date	2012/07/01	Deciphered Date	2014/07/01	HDD/ODD/Card reader/G-Sen		
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Custom	NM-A041					
Date:	Thursday, November 01, 2012		Sheet	36	of	59



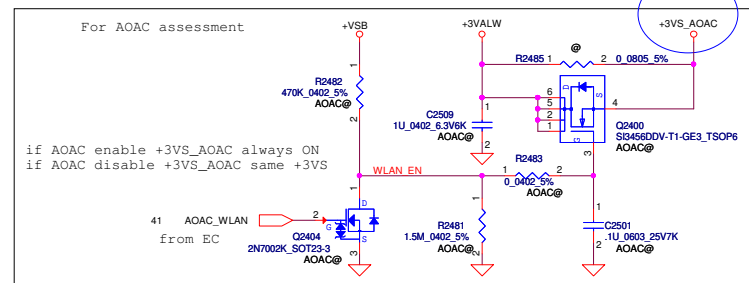
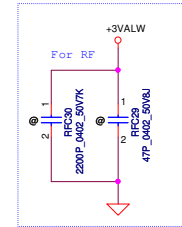
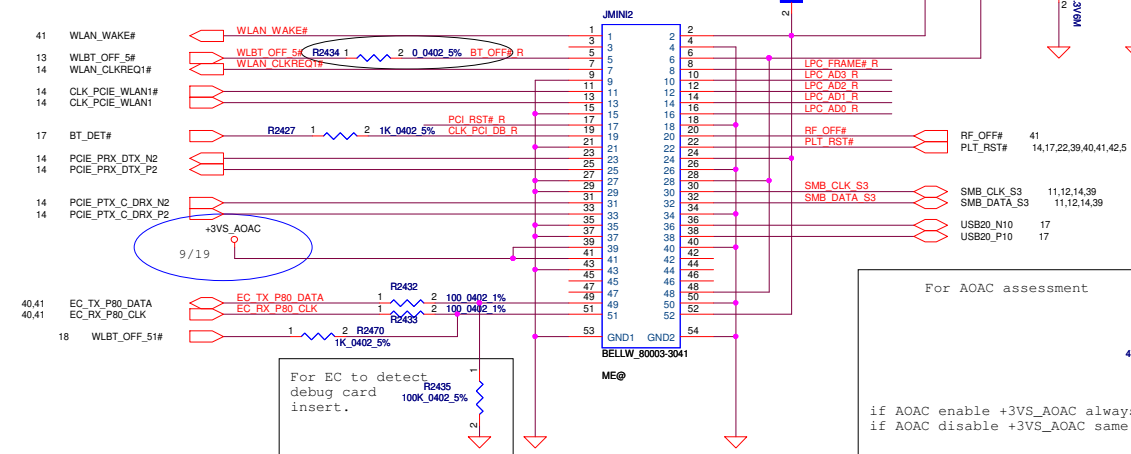
### Mini-Express Card(WLAN)

PN:SP07000JP00

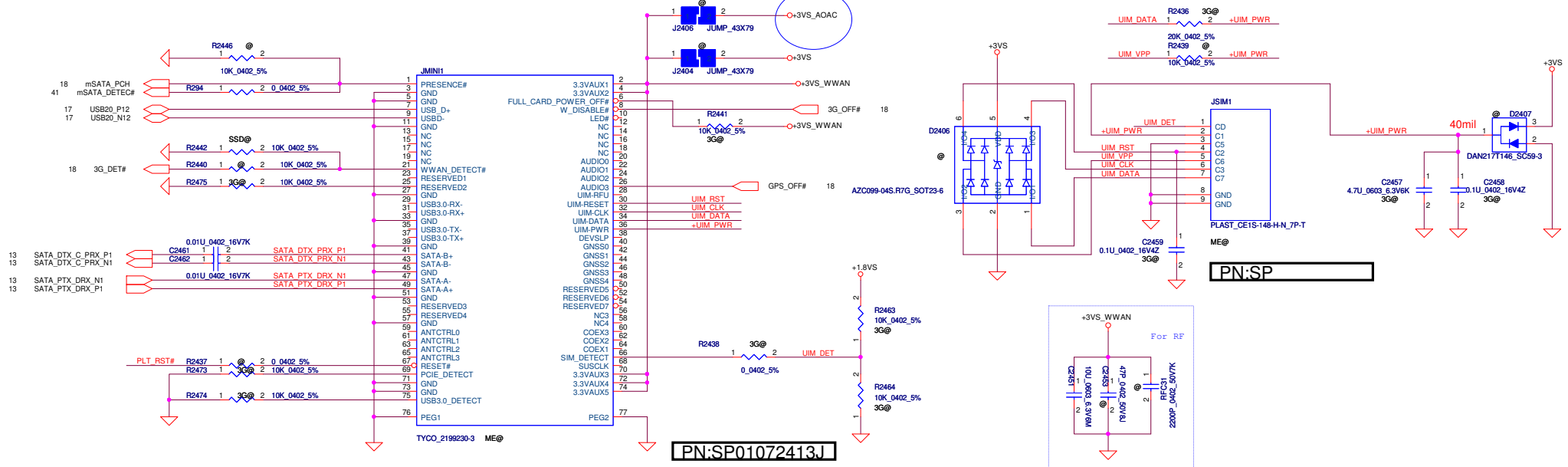
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## BT Connector


Power	Primary Power (mW)	Auxiliary Power (mW)
	Normal	Normal
+3.3V	0	750
+3.3V	430	250 (wake enable)
+1.5VS	500	375
		5 (Not wake enable)



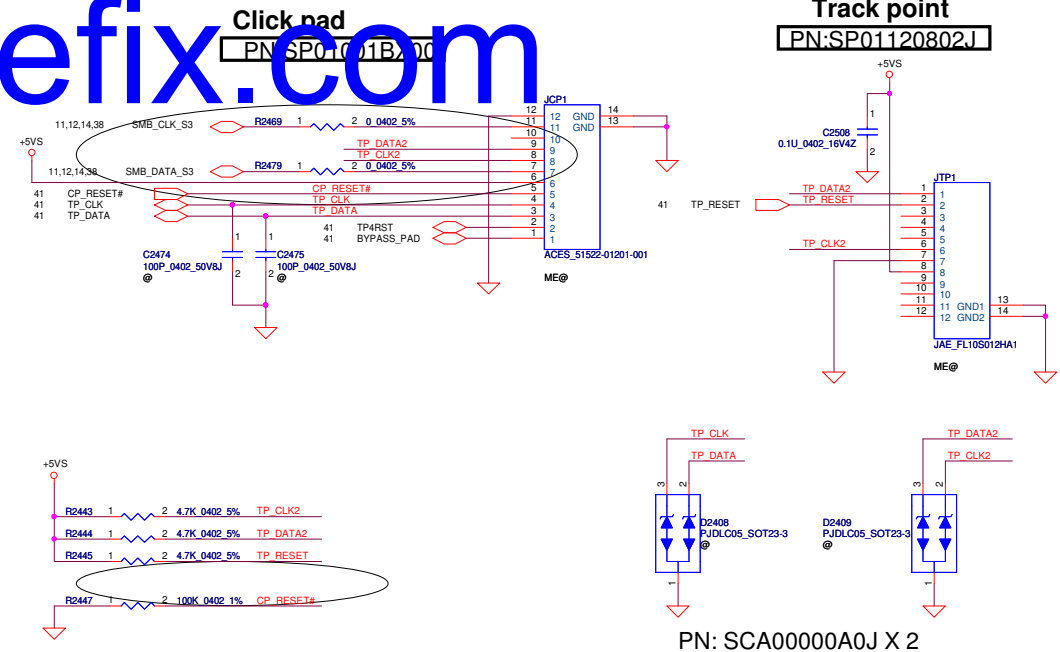
LPC_FRAME# R	R2449	1	2	0	0402	5%	LPC_FRAME#			
LPC_A03 R	R2455	1	2 <td>0 <td>0402 <th>5%</th> <td>LPC_A03</td> <td></td> <td>LPC_FRAME#</td> <td>13,40,41</td> </td></td>	0 <td>0402 <th>5%</th> <td>LPC_A03</td> <td></td> <td>LPC_FRAME#</td> <td>13,40,41</td> </td>	0402 <th>5%</th> <td>LPC_A03</td> <td></td> <td>LPC_FRAME#</td> <td>13,40,41</td>	5%	LPC_A03		LPC_FRAME#	13,40,41
LPC_A02 R	R2456	1	2 <td>0 <td>0402 <th>5%</th> <td>LPC_A02</td> <td></td> <td>LPC_A03</td> <td>13,40,41</td> </td></td>	0 <td>0402 <th>5%</th> <td>LPC_A02</td> <td></td> <td>LPC_A03</td> <td>13,40,41</td> </td>	0402 <th>5%</th> <td>LPC_A02</td> <td></td> <td>LPC_A03</td> <td>13,40,41</td>	5%	LPC_A02		LPC_A03	13,40,41
LPC_A01 R	R2457	1	2 <td>0 <td>0402 <th>5%</th> <td>LPC_A01</td> <td></td> <td>LPC_A02</td> <td>13,40,41</td> </td></td>	0 <td>0402 <th>5%</th> <td>LPC_A01</td> <td></td> <td>LPC_A02</td> <td>13,40,41</td> </td>	0402 <th>5%</th> <td>LPC_A01</td> <td></td> <td>LPC_A02</td> <td>13,40,41</td>	5%	LPC_A01		LPC_A02	13,40,41
LPC_A00 R	R2458	1	2 <td>0 <td>0402 <th>5%</th> <td>LPC_A00</td> <td></td> <td>LPC_A01</td> <td>13,40,41</td> </td></td>	0 <td>0402 <th>5%</th> <td>LPC_A00</td> <td></td> <td>LPC_A01</td> <td>13,40,41</td> </td>	0402 <th>5%</th> <td>LPC_A00</td> <td></td> <td>LPC_A01</td> <td>13,40,41</td>	5%	LPC_A00		LPC_A01	13,40,41
PLT_RST# R	R2459	1	2 <td>0 <td>0402 <th>5%</th> <td>PLT_RST#</td> <td></td> <td>LPC_A00</td> <td>13,40,41</td> </td></td>	0 <td>0402 <th>5%</th> <td>PLT_RST#</td> <td></td> <td>LPC_A00</td> <td>13,40,41</td> </td>	0402 <th>5%</th> <td>PLT_RST#</td> <td></td> <td>LPC_A00</td> <td>13,40,41</td>	5%	PLT_RST#		LPC_A00	13,40,41
CLK_PCI_DB R	R2428	1	2 <td>0 <td>0402 <th>5%</th> <td>CLK_PCI_DB</td> <td></td> <td></td> <td>17,40</td> </td></td>	0 <td>0402 <th>5%</th> <td>CLK_PCI_DB</td> <td></td> <td></td> <td>17,40</td> </td>	0402 <th>5%</th> <td>CLK_PCI_DB</td> <td></td> <td></td> <td>17,40</td>	5%	CLK_PCI_DB			17,40



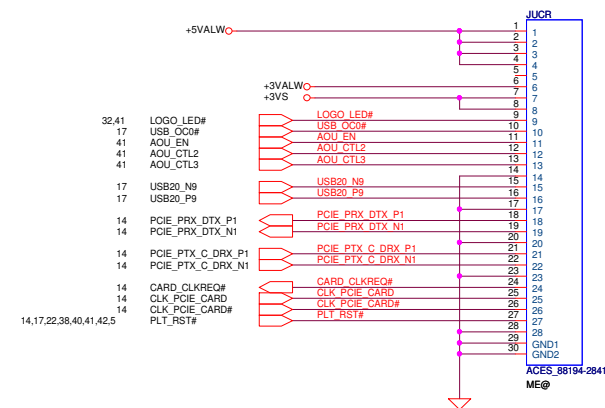
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	PCle-WLAN and WWAN_mSATA			
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Date: Thursday, November 01, 2012						Sheet 38 of 59	


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## Audio+CR Board

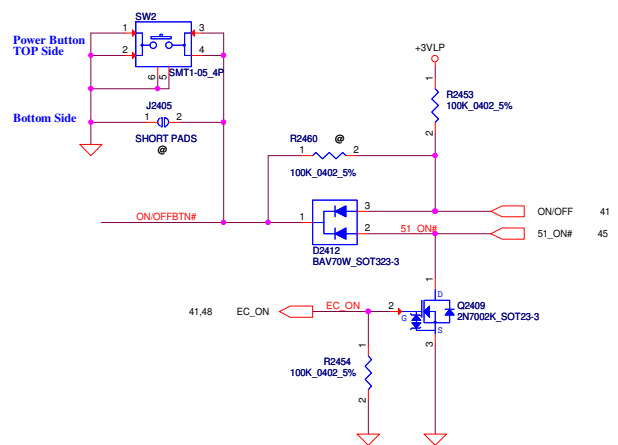


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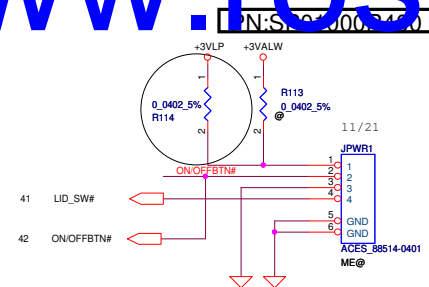
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Issued Date		Deciphered Date		<b>KB/TP/Thermal Sensor/Audio</b>			
2012/07/01		2014/07/01		Size Document Number Custom <b>NW-A041</b>		Rev 1.A	
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ON/OFF switch

Power Button

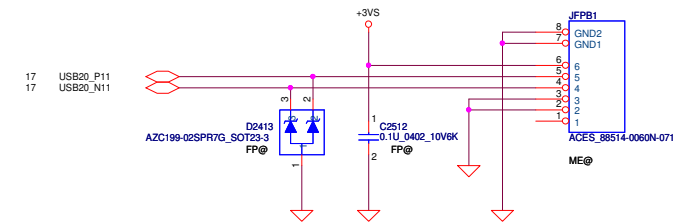


Power Button CONN

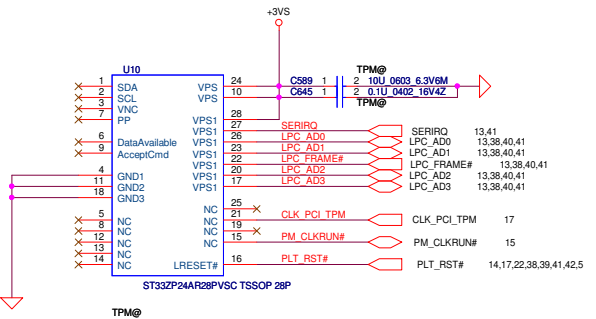


Finger Print Board

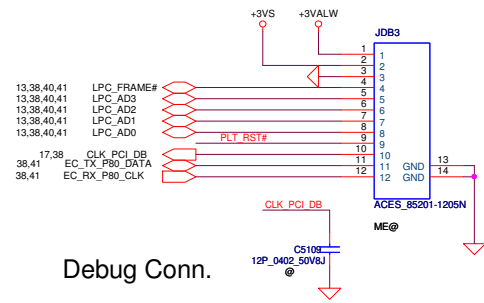
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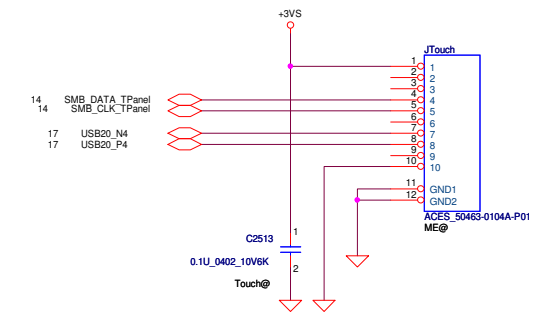
TPM



Debug Conn.




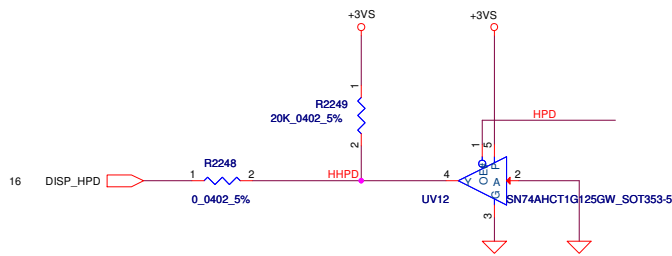
Touch Panel



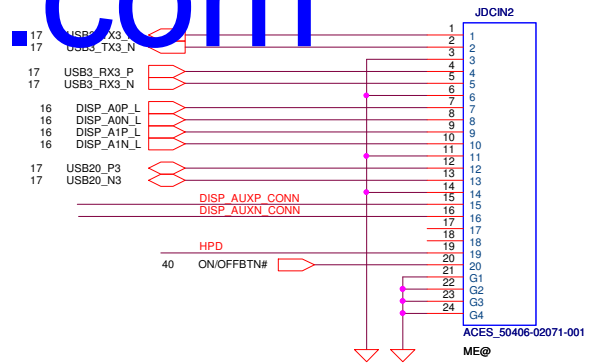
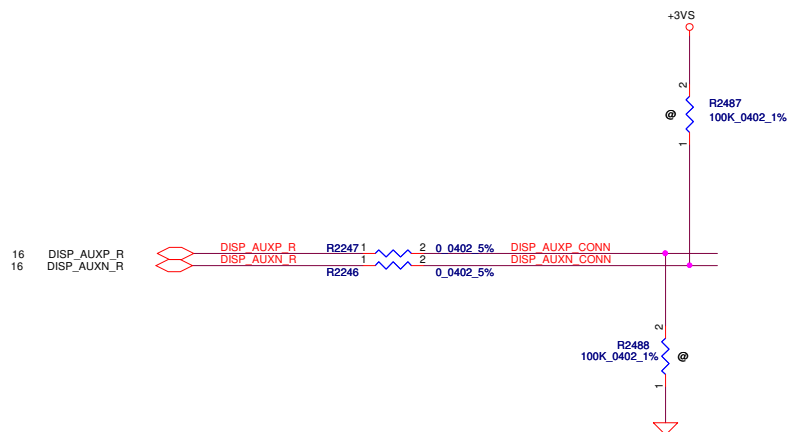




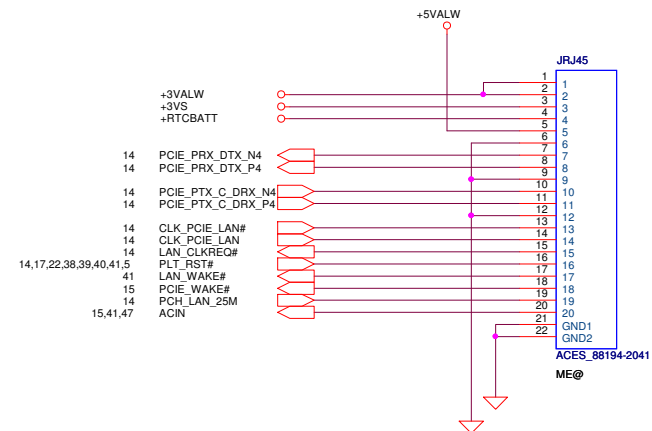
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DP/TMDS Switch Circuit (1)



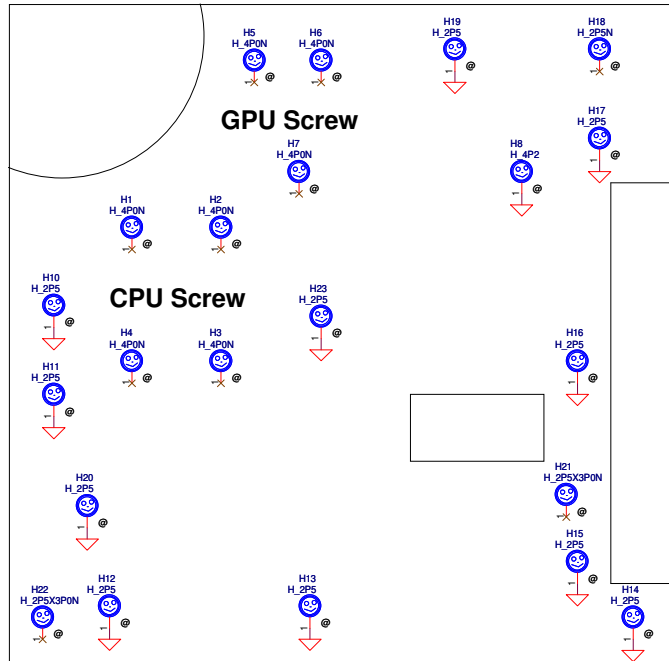
RJ45 Board



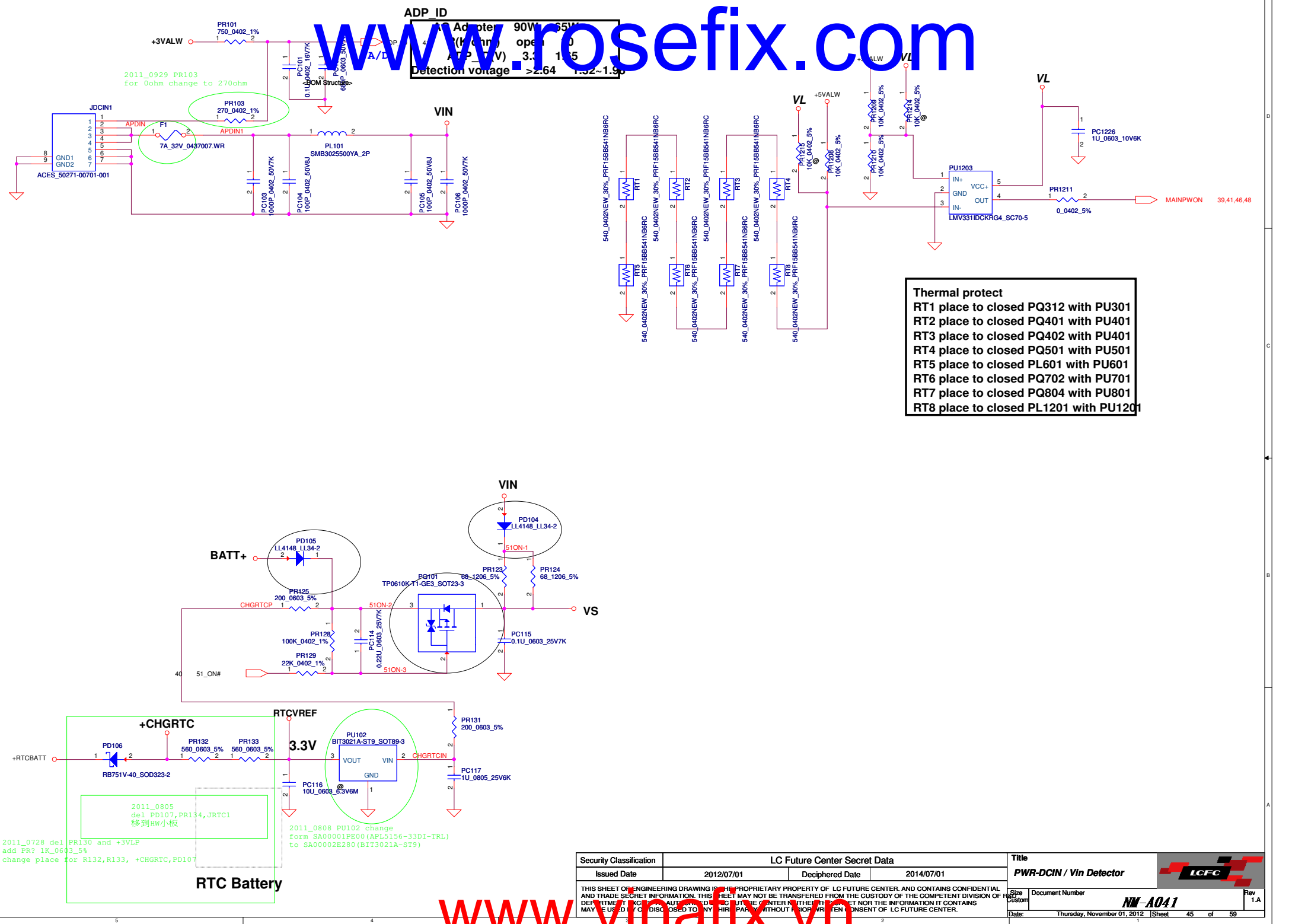
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				Custom	NM-A041	1.A	
				Date:	Thursday, November 01, 2012	Sheet	42 of 59

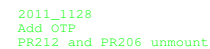
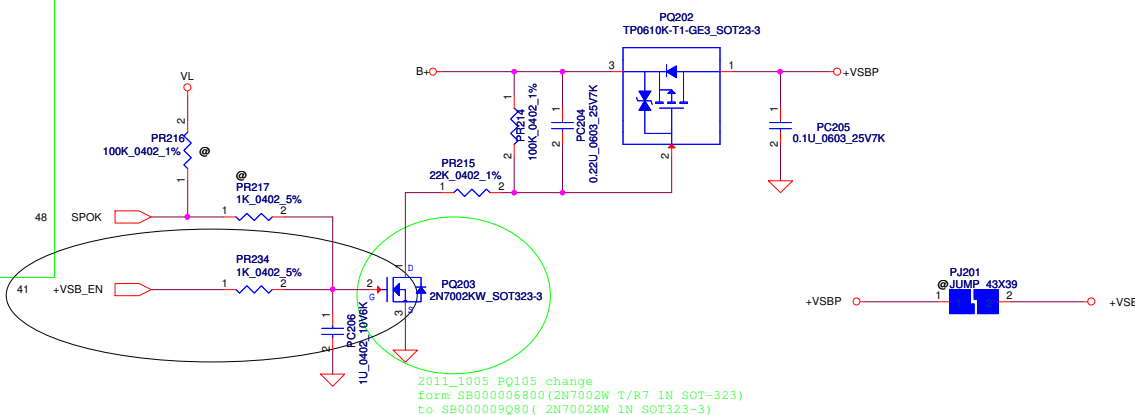


Screw Hole & FD

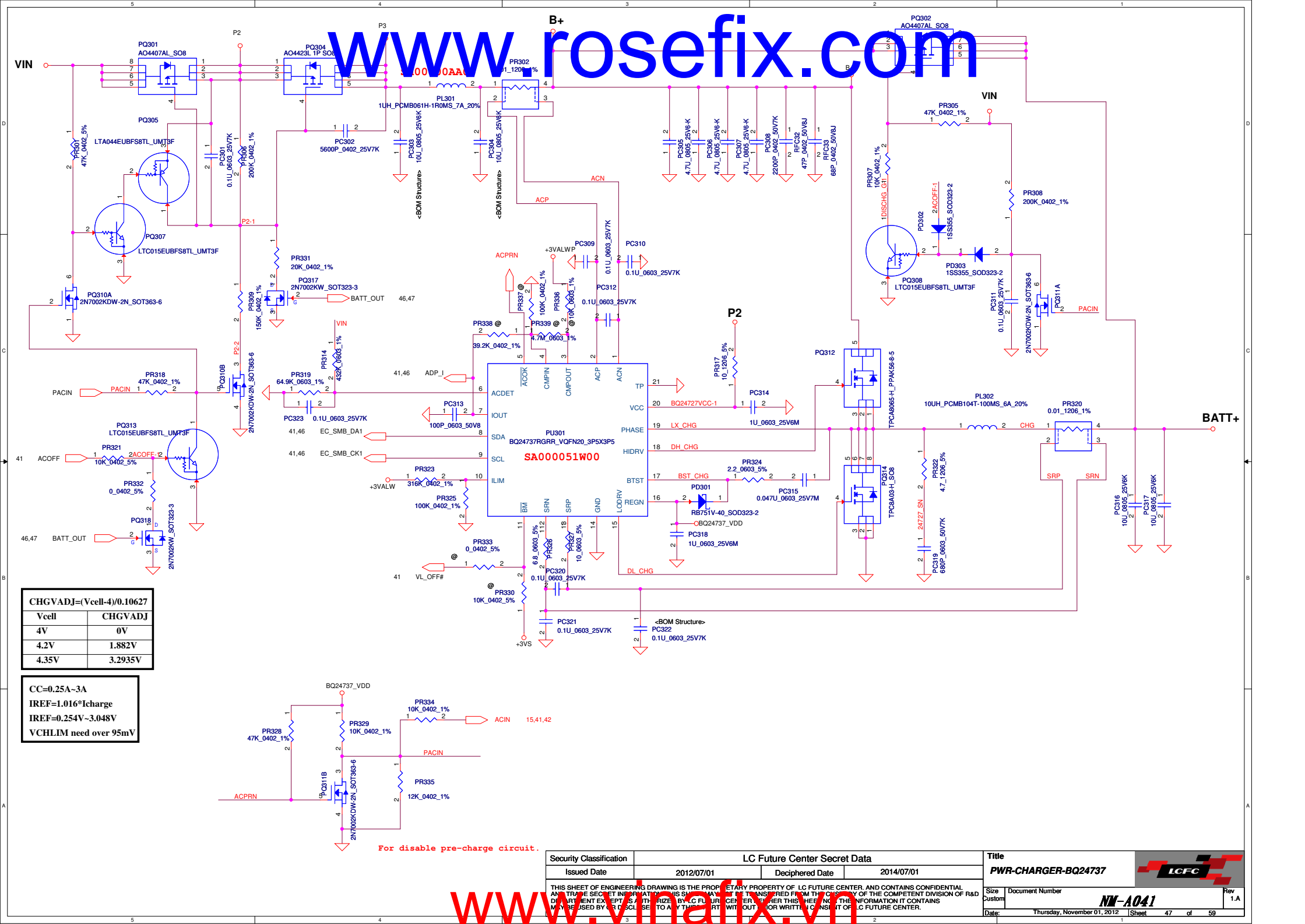


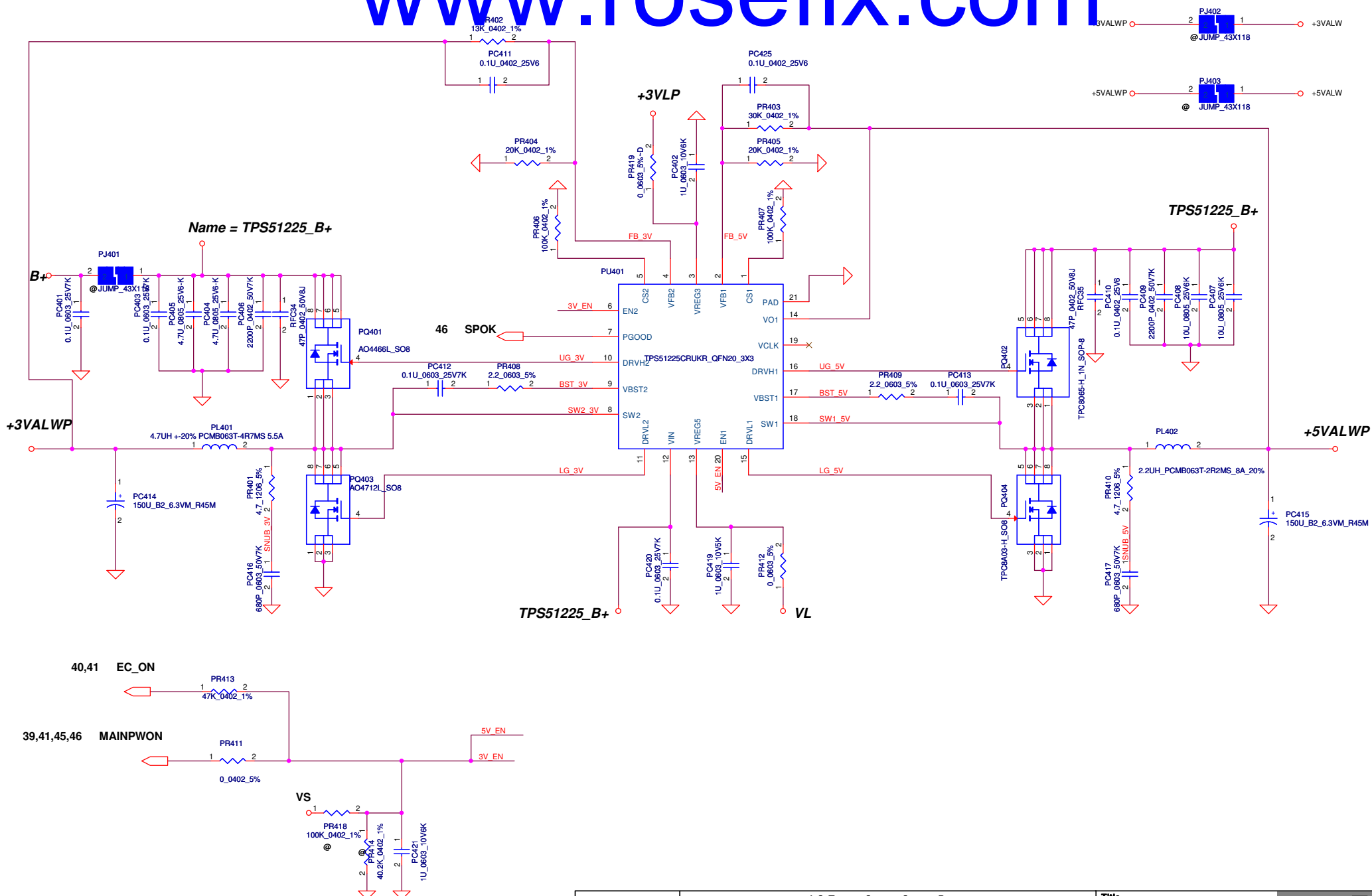
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[illegible]

Title		<b>PWR-BATTERY CONN/OTP</b>			
Size Custom	Document Number			Rev	
	<b>NM-A041</b>			1/J	
Date:	Thursday, November 01, 2012		Sheet	46	of 59

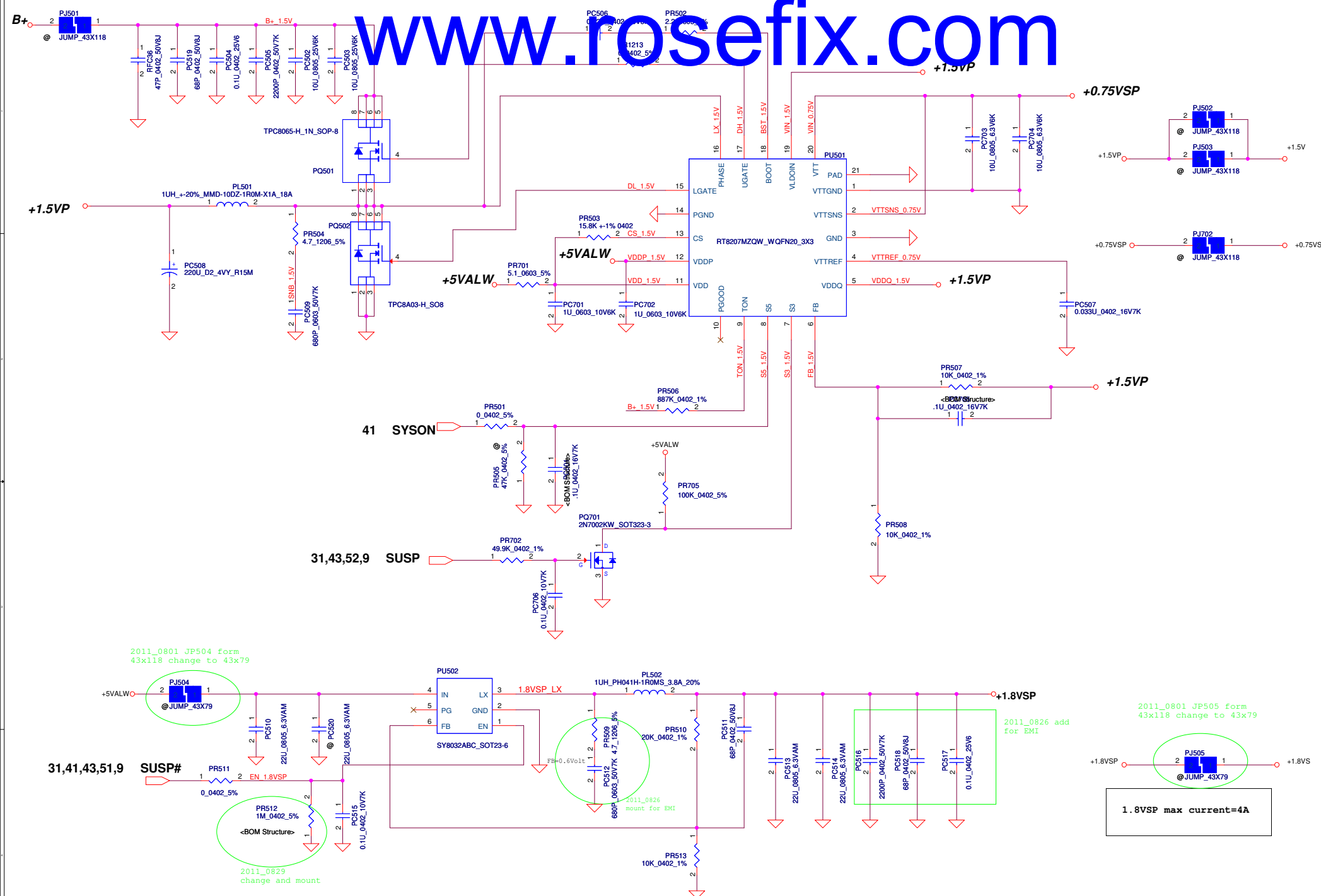




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Title		PWR-3VALWP/5VALWP	
Size	Custom	Document Number	NM-A041
Date	Thursday, November 01, 2012	Sheet	48 of 59

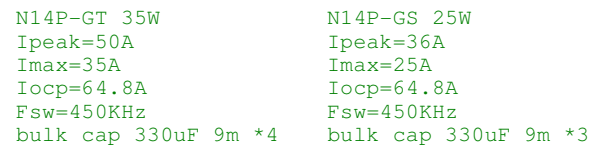




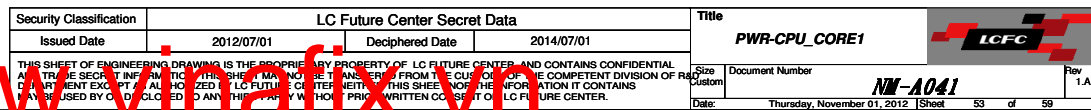
+VCC	SAP
TDC	4.2A
Peak Current	6A
OCF current	7.2A

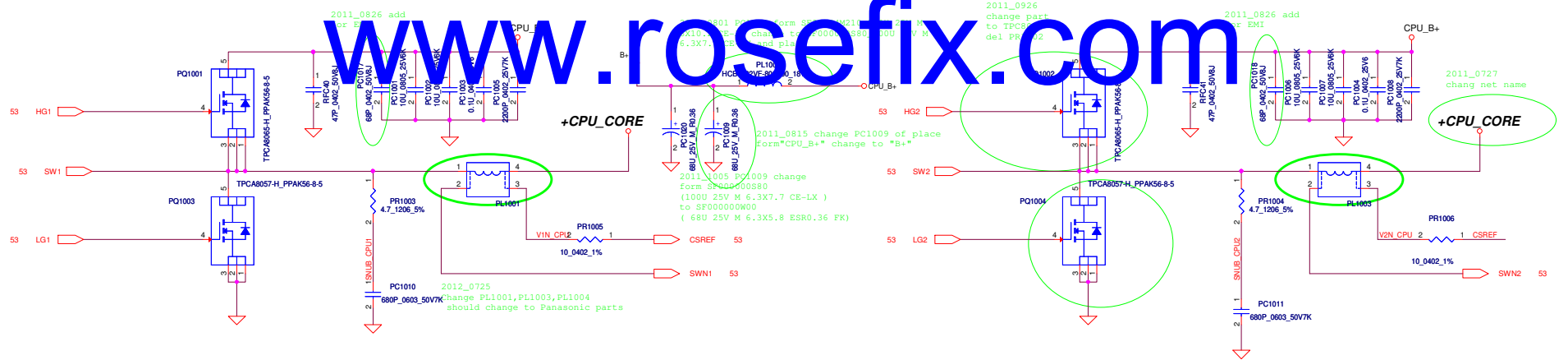


Security Classification		LC Future Center Secret Data		Title <b>PWR+1.05VS_VCCP+0.75VSP</b> 	
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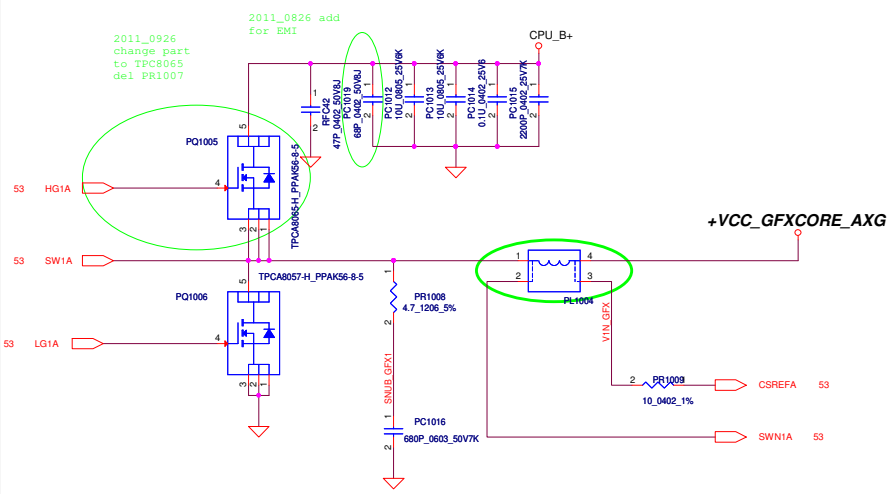
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QC 45W CPU  
VID1=0.9V  
IccMax=94A  
Icc\_Dyn=66A  
Icc\_TDC=52A  
R\_LL=1.9m ohm  
OCP-110A

DC 35W CPU  
VID1=1.05V  
IccMax=53A  
Icc\_Dyn=43A  
Icc\_TDC=36A  
R\_LL=1.9m ohm  
OCP-65A



QC 45W GT2  
VID1=1.23V  
IccMax=46A  
Icc\_Dyn=37A  
Icc\_TDC=38A  
R\_LL=3.9m ohm  
OCP-55A

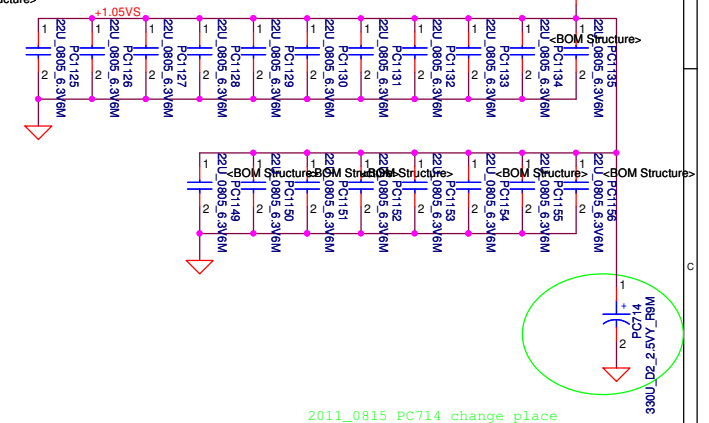
DC 35W GT2  
VID1=1.23V  
IccMax=33A  
Icc\_Dyn=20.2A  
Icc\_TDC=21.5A  
R\_LL=3.9m ohm  
OCP-40A

Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

2011\_0808 place power name change form +V1.05S\_VCCP to +1.05VS

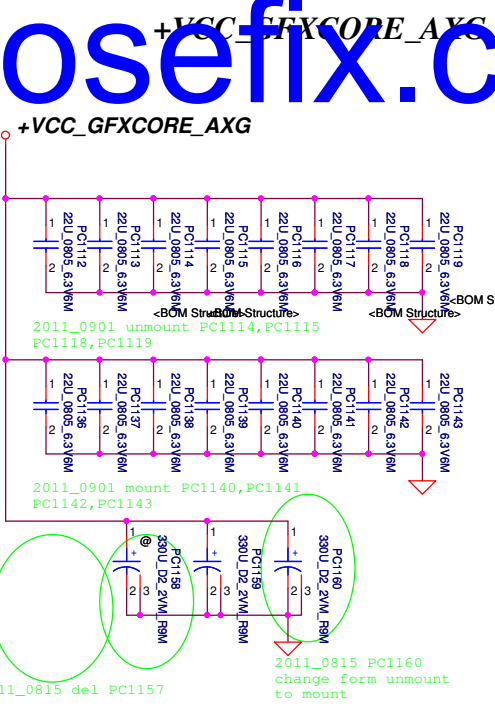
+1.05VS



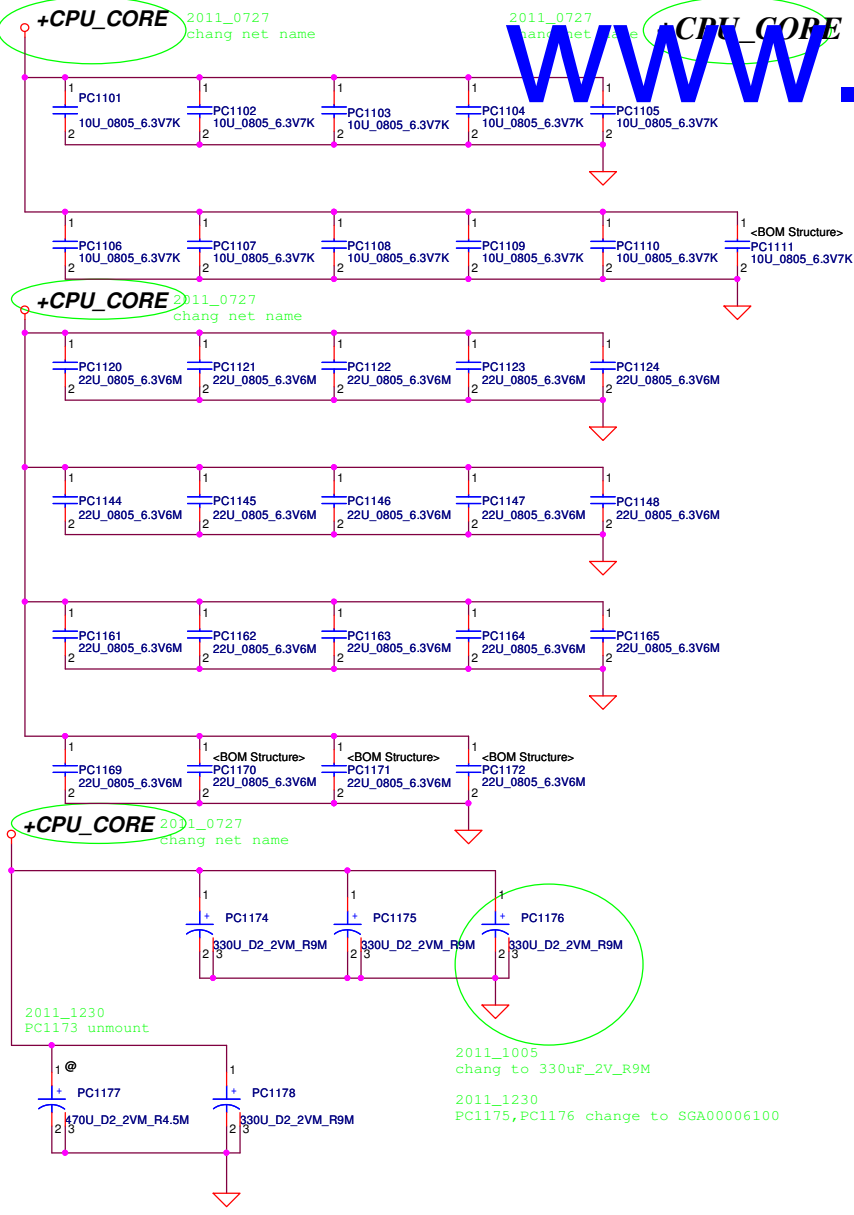
2011\_0815 PC714 change place form "+1.05VS\_VCCPP" to "+1.05VS"

2011\_1005 PC714 change to 330uF\_2V\_R9M

2011\_1007 PC714 form SGA00001Q802 (S POLY C 330U 2V M X LESR6M SX H1.9) change to SGA00002680 (330U\_D2\_2.5V\_R9M)



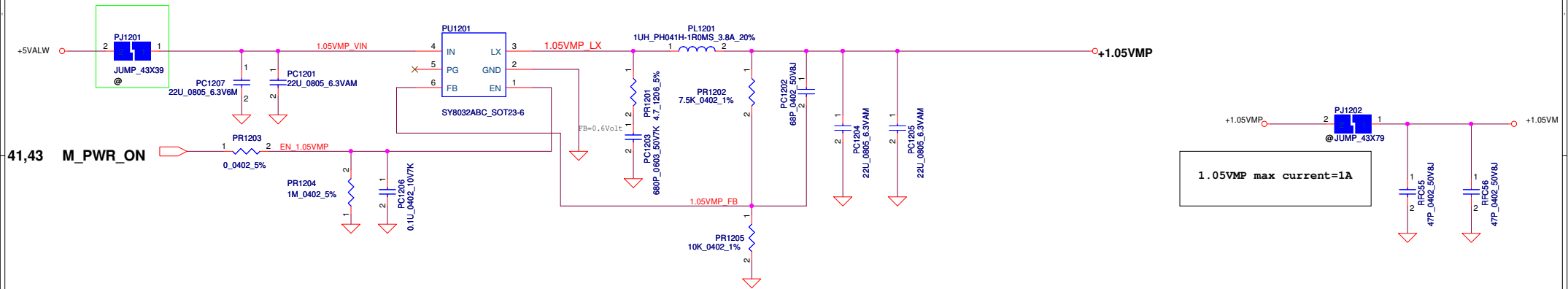
2011\_07929 PC1158 non-mount



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2011\_0923 JUMP form 43X79 change to 43X79







Version change list (P.I.R. List)

Item	Reason for change	PG#	Mocky List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					


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				Date: Thursday, November 01, 2012	Sheet 59 of 59